ABOUT NIT KURUKSHETRA

National Institute of Technology, Kurukshetra (founded as Regional Engineering College, Kurukshetra in 1963) was conferred upon the status of Deemed University on June 26, 2002. Besides B.Tech. & M.Tech. courses, institute offers excellent facilities for advanced research in the emerging areas of Science and Technology leading to Ph.D. degree.

School of VLSI Design and Embedded Systems is offering Ph.D. and M.Tech. programmes in VLSI Design and Embedded System Design. School is equipped with professional EDA tools & sophisticated hardware of Cadence, Synopsys , Mentor Graphics , Xilinx, National Instruments, Intel, Key-pentax Computerized Speech Lab, Freescale. School has signed MoU with SCL (ISRO), Freescale, Europractice. School has been participating in SMDP-C2SD project funded by Ministry of Electronics and Information Technology (MeitY), GoI.

ABOUT CoreEL :

CoreEL Technologies is a Customer Application Specific Product & Solutions (CASPS) company offering INNOVATIVE solutions, which ranges across Intellectual Property (IP) cores, Design & Development, Bespoke System Design & Prototype Development, Next-Gen Digital products, Integrated solutions, Low Volume Manufacturing, System Upgrades and Obsolescence management, EDA tools, COTS products, Semiconductor solutions and Technology Training. CoreEL is a leading developer of advanced electronic system level products and solutions to three primary markets – Aerospace & Defence, Digital Media Broadcast and Universities & Institutions of higher learning.

PATRON

Padmashri Dr. Satish Kumar
Director, NIT Kurukshetra

CONVENER

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MEMBERS

Dr. Shudhanshu Chaudhary (Mob.: 7206550867)
Dr. Gaurav Saini (Mob.: 8950461132)

RESOURCE PERSONS

CoreEL Technology :

- Mr. Ankur Sangal (Sr. Application Engineer)
- Mr. Mayank Singh (Application Engineer)

Registration form should be sent to:

Email: ***nitkkr.sve@gmail.com*** *and*
CC to ***raghav.p@coreel.com***

Website: http://www.nitkkr.ac.in

IMPORTANT DATES

Registration Closes: Sep 8, 2018
Notification about Selection: by Email

" Faculty Development Program in VLSI Design using Xilinx & Mentor Graphics Tools "

(Sep. 10 – 14, 2018)

organized by

National Institute of Technology Kurukshetra

in Association With

CoreEL Technologies
A CASPS Company

National Institute of Technology Kurukshetra (Haryana) 136119-INDIA

REGISTRATION FORM

Name: ……..

Designation:……..

Qualifications: …….

Experience:……Years… …… .Months

Age…… M / F

Organization:……

Address for correspondence:

……

……

Mob……

E-mail:……..

Payment Details:

DD/Cheque No.……..... Date:……

Note: Payment is accepted through Demand Draft / Cheque / or in Cash (on the day of registration).
DD/Cheque must be prepared in favor of Director NIT Kurukshetra

Accommodation required: Yes / No

Signature of Applicant

Signature of Head of Department/Organization with Seal

INTRODUCTION AND OBJECTIVES

VLSI Design is now a most-in-demand area for potential and career conscious engineers. The workshop aims to teach core concepts and impart hands on training of digital IC design and will enable the participants to understand and apply IC related issues of power and performance. It will equip them to implement IC design solutions on FPGAs and using state-of-the-art industrial EDA tools.

WHO CAN APPLY

The proposed FDP is designed for faculty members of Technical institutions, universities, industry persons and PhD/PG scholars.

RESOURCE PERSONS

Resource persons will be invited from CoreEL Technology.

REGISTRATION FEES

Industry/R&D Participants	: Rs. 5000.00
Faculty	: Rs. 3000.00
Outside Research Scholars	: Rs 1200.00
NIT Kurukshetra Participants	: Nil

Student (PhD/PG) participants need to submit scanned copy of a valid proof/ID along with the registration form. Participants will be provided refreshment during the workshop. However, accommodation for outside participants can be arranged on payment basis in institute hostel/guest house subject to the availability. No TA/DA will be paid to the participants. Number of seats are tentatively limited to 30. Scanned copies of duly filled and signed registration form and registration fee payment details (Scanned copy of DD/Cheque) should be sent by email to ***nitkkr.sve@gmail.com*** on or before Sep 8th, 2018. Confirmation to the participants shall be intimated through email within 24 hours.

SCHEDULE

1) Day 1

FPGA design flow using Vivado Hardware required – Basys3/Nexys4DDR

a) 7-Series Architecture Overview
b) Lab 1: Vivado Design Flow
c) Lab 2: Synthesizing a RTL Design
d) Implementation and Static Timing Analysis
e) Lab 3: Implementing the Design

2) Day 2

Hardware required – Basys3/Nexys4DDR

a) IP Integrator
b) Lab 4: Using the IP Catalog and IP Integrator
c) Xilinx Design Constraints
d) Lab 5: Xilinx Design Constraints
e) Hardware Debugging

3) Day - 3

a) Introduction to Embedded System Design using Zynq
b) Create a Vivado project and use IP Integrator to develop a basic embedded system for a target board.
c) Zynq Architecture
d) Extending the Embedded System into Programmable Logic
e) Adding Peripherals in Programmable Logic

4) Day - 4

a) Introduction to IC/ASIC Design Flow and Mentor EDA Tools.
b) Detailed Semi-Custom IC Design Flow.
c) Hands-On Lab Sessions.

5) Day - 5

a) Detailed Semi-Custom IC Design Flow (Contd)
b) Hands-On Lab Sessions.
c) Detailed Full-Custom IC Design Flow.
d) Hands-On Lab Sessions