SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Scheme for M.Tech (Embedded Systems)

First Semester

Sl. No.	Course No.	Subject	L-T-P	Credits
1	**SVE511T**	Embedded System Fundamentals	**3-0-0**	3
2	**SVE531T**	Embedded System Software Development	**3-0-0**	3
3	**SVE505T**	Hardware Description Languages and FPGA based Design	**3-0-0**	3
4		Elective-1	**3-0-0**	3
5		Elective-2	**3-0-0**	3
6	**SVE537P**	Embedded Systems Lab	**0-0-4**	2
7	**SVE539P**	Seminar	**0-0-2**	1

Total Credits = 18

Semester-I Electives

	Elective-1
1	Fault Tolerant Digital System Design (**SVE541T)**
2	Introduction to MEMS **(SVE515T)**
3	Data Compression**(ECE115T)**
4.	Hardware Algorithms for Computer Arithmetic **(SVE519 T)**
	Elective-2
1	Reconfigurable Computing**(SVE547T)**
2	Digital Signal Processing **(ECE501T)**
3	Digital CommunicationSystems **(ECE503T)**
4	Digital IC Design **(SVE501T)**

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Second Semester

Sl. No.	Course No.	Subject	L-T-P	Credits
1	**SVE512T**	Real Time Systems	3-0-0	3
2	**SVE532T**	Hardware Software Co-design	3-0-0	3
3		Elective-1	3-0-0	3
4		Elective-2	3-0-0	3
5		Elective-3	3-0-0	3
6	**SVE534P**	Design Lab	0-0-4	2
7	**SVE536P**	Seminar	0-0-2	1

Total Credits = 18

Semester-II Electives

	Elective-1
1	Algorithms to Architectures (**SVE508T)**
2	Wireless Sensor Networks (**MECE-205)**
3	RF Micro-electronics(**SVE512T)**
	Elective-2
1	Mixed Signal IC Design (**SVE500T)**
2	Low Temperature Co-fired Ceramics Technology (**SVE546T)**
3	Computer Based Control Systems(**SVE514T)**
	Elective-3
1	Low Power VLSI Design (**SVE510T)**
2	Digital Signal processing with FPGAs(**SVE522T)**
3	Embedded Microcontrollers and applications (**SVE524T)**

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Third Semester

Sl. No.	Course No.	Subject	L-T-P	Credits
1	**SVE601P**	Preparatory Work for Dissertation	0-0-20	10
			20	**10**

Total Credits = 10

NOTE-I: (**Semester-III).**

The Preparatory Work for Dissertation shall be evaluated by a committee comprising the following [on the basis of one mid semester seminar and one end semester seminar presented and one end semester report submitted by the candidate].

1) HOD or faculty nominee proposed by HOD.
2) Dissertation Supervisor (and co-supervisor)
3) Two senior most faculty members of the department.

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Fourth Semester

Sl. No.	Course No.	Subject	L-T-P	Credits
1	**SVE602P**	Dissertation	0-0-32	16

Total Credits = 16

NOTE-II:(Semester – IV)

(i) The Dissertation shall be evaluated by a committee comprising the following through a presentation cum viva-voce examination.

1) HOD or faculty nominee proposed by HOD.
2) Dissertation Supervisor (and co-supervisor)
3) One external expert appointed by the Department

(ii) For award of grade, following criteria to be used.

Grade Awarded	Conditions to be fulfilled
A+	One paper accepted/published in SCI Journal
A	One good quality paper accepted/published in non-paid journal or two good quality papers presented in international / national conference.*
B	One good quality paper presented in international conference
C/D	In other cases

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
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Embedded System Fundamentals

(SVE511T)

An Introduction to Embedded Systems : An Embedded System, Processor in the System, Other Hardware Units, and Software Embedded into a System, Exemplary Embedded Systems, Embedded System – On- Chip (SOC) and in VLSI Circuit.

Processor and Memory Organization: Structural Units in a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded Systems, Allocation of Memory to Program Cache and Memory Management Links, Segments and Blocks and Memory Map of a System, DMA, Interfacing Processors, Memories and Input Output Devices.

Devices and Buses for Device Networks: I/O Devices, Timer and Counting Devices, Serial Communication Using the "1^2C" (Inter IC) CAN (controller area network), Profibus Foundation Field Bus and Advanced I/O Buses Between the Network Multiple Devices. Host Systems or Computer Parallel Communication between the Networked I/O Multiple Devices using the ISA, PCI, PCI-X and Advanced Buses.

Device Drivers and Interrupts Servicing Mechanics: Device Drivers, Parallel Port and Serial Prot Device Drives in a System, Device Drovers for Internal Programmable Timing Devices, Interrupt Servicing Mechanism.

Programming Concepts and Embedded Programming in C, C++, VC++ and JAVA: Interprocess Communication and Synchronization of Processes, Task and Threads, Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Interprocess Communication.

Hardware-Software Co-design in an Embedded System: Embedded System Project Management Embedded System Design and Co-Design issues in System Development Process.

Design Cycle in the Development Phase for an Embedded System: Use of Target Systems, Use of Software Tools for Development of an Embedded System, Use of Scopes and Logic Analysis for System, Hardware Tests, Issues in Embedded System Design.

Text Books:

Raj Kamal, "Embedded Systems: Architecture, Programming and Design", TMH.

David Simon, "An Embedded Software Primer", Pearson Education.

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M.Tech. (Embedded Systems)

Embedded System Software Development

(SVE531T)

Real-time and embedded systems; software issues in embedded systems; software development process.

Requirement analysis; use cases, identification and analysis of use cases, use case diagrams.

Design; Architectural design, design patterns and detailed design; implementation; languages , compilers, run-time environments and operating systems for embedded softwares.

Testing; methodologies and test cases.

Text Book and References:

1. Philip Koopman**,"**Better Embedded System Software", Drumnadrochit Education LLC.
2. Mani Srivastava, Vijay Raghunathan, "Embedded Computing: A Systems Approach
3. David E. Simon, "An Embedded Software Primer"

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Hardware Description Languages And FPGA Based Design (SVE505T)

Verilog : basic concepts- Lexical conventions, data types, system tasks and compiler directives. Modules and ports. Gate level modeling- gate types, various types of gate delay specifications. Data flow modeling- assignments, delays, expressions, operators, . Behavioral modeling- structured procedures, procedural assignments, timing controls, conditional statements, loops, sequential and parallel blocks, generate blocks. Tasks and functions. Describing Clock driven Finite-State Machines, Event driven Finite State Machines,. Switch level modeling.
Verilog Synthesis for FPGA Implementation: Verilog constructs and operators, interpretation of Verilog constructs, synthesis design flow- RTL to gates, translation, un-optimized intermediate representations, logic optimization, technology mapping and optimization, technology library, design constraints, optimized gate level description.

Microprocessor Design: History of Microprocessors, Instruction Set Design , Addressing Modes Data Flow: Zero-,One-, Two- or Three-Address Design Register File and Memory Architecture , Operation Support ,FPGA Microprocessor Cores ,Hardcore Microprocessors Softcore Microprocessors , Case Studies, Nios-Processor Design .

FPGA Architectures and Technology. Historical background, FPGA Technology ,Classification by Granularity, Classification by Technology, Benchmark for FPLs, Xilinx, Altera, Actel, LaticeFPGAs- Recent developments- new architectures of FPGAs, field programmable interconnect.Reconfigurable logic, Partial Reconfiguration.

TEXT BOOKS:
S. Palnitkar, Verilog HDL : A Guide to Digital Design and Synthesis, PH/Pearson,
K. Coffman, Real World FPGA Design with Verilog, PH,
REFERENCE BOOKS:
R. C. Seals and G. F. Whapshott, Programmable Logic : PLDs and FPGAs, MH.
A,K. Sharma, Programmable Logic Handbook : PLDs, CPLDs and FPGAs, MH.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Fault Tolerant Digital System Design
(SVE541T)

Basic Concepts: Reliability, Failures and faults, Reliability and failure rate,Relation Between reliability & mean time between failure, maintainability &Availability Reliability of Series and parallel Systems.

Test Generation: Fault diagnosis of digital Systems, Test generations forcombinational logic circuits – conventional methods, Random testing, transitioncount testing and signature analysis.

Fault Tolerant Design – I : Basic concepts – static, dynamic, hybrid, and self –purging redundancy, Sift – out Modular redundancy (SMR) ,triple modularredundancy, 5MR reconfiguration, use of error correcting codes.

Fault Tolerant Design – II : Time redundancy, software redundancy, fail – softoperation , examples of practical fault tolerant systems, introduction to fault tolerantdesign of VLSI chips.

Self Checking Circuits: Design of totally self checking checkers , checkers using m-out of n codes, Berger codes and low cost residue code, self – checking sequentialmachines, partially self – checking circuits.

Fail safe Design: Strongly fault secure circuits, fail – safe design of sequentialcircuits using partition theory and Berger codes, totally self – checking PLA design.

Design for testable combination logic circuits: Basic concepts of testability,controllability and observability. The Read – Muller expansion technique, level OR-AND-OR design, use of control and syndrome – testable design.

Testable Design of Sequential Circuits : The scan – path technique, level – sensitivescan design (LSSD) and random Accers scan technique, built – in – test, built – in –test of VLSI chips, design for autonomous self – test, design in testability into logicboards.

BOOKS:
1. Parag K. Lala : Fault Tolerant & Fault Testable Hardware design, (PHI).
2. Parag K LaLA : Digital Systems design using PLD’s (PHI).
3. N.N. Biswas :Logoc Design Theory (PHI).

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Introduction to MEMS

(SVE515T)

Introduction, Basic Structures of MEM Devices: (Canti Levers, Fixed Beams diaphragms).Broad Response of Micro Electromechanical Systems (MEMs) to Mechanical (force, pressure etc.) Thermal, Electrical, Optical and Magnetic Stimuli, Compatibility of MEMS from the point of Power Dissipation, Leakage etc.

Review of Mechanical Concepts: Stress, Strain, Bending Moment, Deflection Curve. Differential Equations Describing the Deflection under Concentrated Force, Distributed Force, Deflection Curves for Canti Levers – Fixed Beam. Electrostatic Excitation – Columbic Force between the Fixed and Moving Electrodes. Deflection with Voltage in C.L, Deflection Vs Voltage Curve, Critical Fringe Fields – Field Calculations using Laplace Equation. Discussion on the Approximate Solutions - Transient Response of the MEMS.

Two Terminal MEMS: Capacitance Vs Voltage Curve – Variable Capacitor. Applications of Variable Capacitors. Two Terminal MEM Structures.Three Terminal MEM Structures – Controlled Variable Capacitors – MEM as a Switch and Possible Applications.

MEM Circuits & Structures for Simple Gates: AND, OR, NANO, NOR , Exclusive OR, simple MEM Configurations for Flip-Flops Triggering, Applications to Counters, Converse Applications for Analog Circuits like Frequency Converters, Wave Shaping. RF Switches for Modulation. MEM Transducers for Pressure, Force Temperature.Optical MEMS.

MEM Technologies: Silicon Based MEMS- Process Flow- Brief Account of Various Processes and Layers like Fixed Layer, Moving Layers, Spacers Etc. Etching Technologies. Metal Based MEMS: Thin and Thick Film Technologies for MEMS. PROCESS flow and Description of the Processes.Status of MEMS in the Current Electronics scenario.

Text Book/References:

1. Gabriel M.Review, “R.F. MEMS Theory, Design and Technology”, John Wiley & Sons.
2. ThimoShenko, “Strength of Materials”, CBS Publishers & Distributors.
3. Ristic L.(Ed.), “Sensor Technology and Devices”, Artech House, London.
4. ServeyE.Lyshevski, “MEMS and NEMS, Systems Devices; and Structures”, CRC Press.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Data Compression

(ECE115T)

Introduction**:** Brief history of data compression applications, Overview of information theory and redundancy, Human audio - visual systems, Taxonomy of compression techniques. Overview of source coding, source models, scalar quantization theory, rate distribution theory, vector quantization. Evaluation techniques- error analysis and methodologies.

Text Compression**:** Compact techniques-Huffmann coding-arithmetic coding-Shannon-Fano coding and dictionary techniques-LZW family algorithms. Entropy measures of performance-Quality measures.

Audio compression techniques, filtering, basic subband coding, application to speech coding, G.722, application to audio coding, MPEG audio, progressive encoding for audio silence compression.

Image Compression

Predictive techniques-PCM, DPCM, DM. Contour based compression- quad trees, EPIC, SPIHT, Transform coding, JPEG, JPEG-2000

Video Compression

Video signal representation, Video compression techniques-MPEG, Motion estimation techniques-H.261. Overview of Wavelet based compression and DVI technology, Motion video compression.

REFERENCES :

1. Mark Nelson, “Data compression book”, BPB Publishers, New Delhi.
2. Peter D. Symes – “Video compression” , McGrawHill.
3. N.Jayant – “Signal compression - coding of Speech, Audio, Text, Image and Video”, world scientific.
4. Sayood Khaleed, “Introduction to data compression”, Morgan Kauffman, London.
5. Watkinson, J. “Compression in video and audio”, Focal press, London.
6. Jan Vozer, "Video compression for multimedia”, AP profes, NewYork.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Hardware Algorithms For Computer Arithmetic
(SVE519T)

Review of Number systems, their encoding and basic arithmetic operations, Class of Fixed-Radix Number Systems, Unconventional fixed-point number systems, Representing Signed Numbers, Negative-radix number Systems, Redundant Number Systems, Residue Number Systems.

Manchester carry chains and adders, Carry-Look-ahead Adders, Carry determination as prefix computation, Alternative parallel prefix networks, VLSI implementation aspects, Variations in Fast Adders, Simple carry-skip and Carry-select adders, Hybrid adder designs, Optimizations in fast adders, Multi-Operand Addition, Wallace and Dadda trees, Parallel counters, Generalized parallel counters, Adding multiple signed numbers.

Shift/add multiplication algorithms, Programmed multiplication, Basic hardware multipliers, Multiplication of signed numbers, Multiplication by constants, Preview of fast multipliers, High-Radix Multipliers, Modified Booth's recoding, Tree and Array Multipliers, Variations in Multipliers,

Shift/subtract division algorithms, Programmed division, Restoring hardware dividers, Non-restoring and signed division, Division by constants, Preview of fast dividers, High-Radix Dividers, Variations in Dividers, Combined multiply/divide units, Hardware implementation.

Floating-point arithmetic operations, Rounding schemes, Logarithmic number systems, Floating-point adders, Barrel-shifter design, Leading-zeros/ones counting, Floating-point multipliers, Floating-point dividers, Arithmetic Errors and Error Control.

Square-Rooting Methods, The CORDIC Algorithms, Computinglogarithms, Exponentiation, Approximating functions, Merged arithmetic, Arithmetic by Table Lookup, Tradeoffs in cost, speed, and accuracy.

REFERENCES:

1. Parhami, B., Computer Arithmetic: Algorithms and Hardware Design, Oxford University Press.
2. Koren, I., Computer Arithmetic Algorithms, 2nd Edition, Uni Press.
3. Ercegovac, M. and Lang, T., Digital Arithmetic, Elsevier.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Reconfigurable Computing
(SVE547T)

Reconfigurable Computing Hardware: Device Architecture, Reconfigurable Computing Architecture, Reconfigurable Computing Systems

Programming Reconfigurable Computing Systems: Compute model and System Architectures, Programming FPGA Application in VHDL, Compiling C in Spatial Computing, Operating System support for Reconfigurable.

Case Studies of FPGA Applications: Dynamic and Static Reconfigurable Design, ATR (Access to Recovery) Implementation, Logic Emulation: Uses and Types

Implication of Floating Point for FPGA: Floating Point Implication Case Studies, Hardware/Software Portioning and Partial Evaluation, Systolic Architectures.

REFERENCES:

1. Morgan Kaufmann's Reconfigurable Computing
2. Scott Hauck, Andre DeHon: Reconfigurable Computing: The Theory and Practice of FPGA Based Computation

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Digital Signal Processing
(ECE501T)

DFT & FFT

Frequency-Domain Sampling- The Discrete Fourier Transform: Frequency-Domain sampling and reconstruction of Discrete-Time Signals, Discrete Fourier Transform, DFT as a linear transformation, Relationship of the DFT to other transforms. Properties of the , Use of the DFT in linear filtering, Filtering of long data sequences. The Discrete Cosine Transform, FFT Algorithms**,** Divide-and-conquer approach to computation of the DFT, Radix-2 , Radix-4, and Split-Radix FFT algorithms. Applications of FFT Algorithms.

Filter Structures & Design
Direct-form Cascade-form Frequency-sampling and Lattice structures for FIR filters.
Direct-form, Signal flow graphs and transposed structures for IIR filters. Cascade and Parallel form structures, Lattice and lattice-ladder structures for IIR systems.
Causality and its implications, Characteristics of practical frequency selective filters.Symmetric and anti-symmetric FIR filters, Design of linear-phase FIR filters using windows, by frequency-sampling method. Design of optimum equiripple linear-phase FIR filters.
Design of IIR Filters from Analog Filters,IIRfilter design by approximation of derivatives, bilinear transformation, and impulse invariance.Characteristics of commonly used analog filters.

Multirate Digital Signal Processing
Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D. Polyphase filter structures, Design of phase shifters, Interfacing of digital systems with different sampling rates, Implementation of narrowband lowpass filters, Subband coding of speech signals. Two-Channel and M-Channel QMF BanksElimination of aliasing, Condition for perfect reconstruction, Polyphase form of the QMF bank.

Linear Prediction and Adaptive Filters
Rational power spectra, Relationships between the filter parameters and the autocorrelation sequence. Forward linear prediction, backward linear prediction, Optimum reflection coefficients for the lattice forward and backward predictors, Relationship of an AR process to linear prediction. AR lattice structure, ARMA processes and lattice-ladder filters.
Wiener Filters for Filtering and Prediction, Applications of Adaptive Filters**,** Minimum mean-square-error criterion, LMS algorithm, Related stochastic gradient algorithms.

REFERENCES:

1. Roman Kuc: Introduction to Digital Signal Processing. MGH
2. JG Proakis: Digital Signal Processing PHI.
3. Oppenheim Schafer: Discrete Time Signal Processing. PHI
4. Simon Haykin, Adaptive Filter Theory, PTH

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Digital Communication Systems
(ECE503T)

Characterization of Communication Signals & Systems

Representation of Band pass Signal and System: Response of a band pass system to band pass signal, Representation of band pass stationary stochastic processes.

Representation of digitally modulated signals**:** memory less modulation methods, Linear modulation with memory, Nonlinear modulation methods with memory.

Spectral Characteristics of Digitally Modulated Signals**:** Power spectra of Linearly modulated Signals, CPFSK and CPM Signals, Modulated Signals with memory.

Band pass Modulation & Demodulation

Digital Band Pass Modulation techniques, Detection of signals in Gaussian noise,

Coherent Detection**:** Coherent Detection of PSK, MPSK and FSK and its error performance, Sampled Matched Filter

Non Coherent detection**:** Detection of DPSK, FSK, Binary Differential PSK and their error performance, required tone spacing for non coherent orthogonal FSK. Comparison of bit error performance of various modulation techniques.

M-ary Signaling & Performance, Symbol Error Performance for M-ary Systems; MPSK and MFSK, Bit Error probability versus symbol error probability.

Digital Signaling Over a Channel WithIntersymbol Interference

Signal design for band limited channels. Communication through Band limited Linear Filter Channels: optimum demodulation for ISI and additive white Gaussian noise**,** Linear equalization: Peak distortion Criterion, Mean Square Error Criterion, Performance Characteristics of MSE Equalizer, Decision-Feedback equalization: Coefficient Optimization, Performance Characteristics

Spread Spectrum Techniques:

Spread Spectrum Overview: Attributes of SS Systems, Spreading Techniques, Model for DS SS Interference Rejection, Pseudonoise Sequences, DSSS Systems: Processing Gain and Performance**,** Frequency Hopping Systems**:** FH with diversity, Fast hopping versus Slow hopping, FFH Demodulator, Processing Gain, Synchronization**:**Acquition and Tracking, Jamming Considerations and Applications.

REFERENCES:

1. Simon Haykin: Communication System, Wiley Eastern Limited. .
2. J.Dass, SK Mullick& PK Chatterjee: Principle of Digital Communication, Wiley Eastern Limited.
3. Martin S. Roden :Digital and Data Communication System P.H.Inc, London, .
4. Viterbi, A.J. and J.K. Omura :Principles of Digital Communication, Mc-Graw Hill Book Company, New York.
5. Bernard Sklar: Digital Communications, Fundamentals & Applications, Pearson

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Digital IC Design
(SVE501T)

Modeling of Interconnects: Interconnect parameters, wire models, SPICE models for wires.
CMOS Inverter: Static and Dynamic Behavior, Power, Energy and Energy Delay, Technology scaling and its impact.
Design of CMOS Combinational Logic Gates: Static and dynamic CMOS Design, Speed and power dissipation in dynamic circuits, cascading of gates, designing logic for reduced supply voltages, simulation of logic circuits.
Design of CMOS Sequential Logic Circuits: Static and dynamic latches and registers, alternative register styles, pipelined sequential circuits, non-bistable sequential circuits.
Custom, Semi-custom, and Structured array design approaches: Cell Based Design – standard, compiled , macro cells, mega cells, ArrayBased Design – mask programmable and rewired arrays.
Coupling with Interconnects: Effects of Interconnect Parasitics, Advanced Interconnect techniques.
Timing issues in Digital Circuits: Timing classification, synchronous timing basics, sources of skew and jitter, clock distribution techniques, latch-based clocking, Self-timed circuit design, synchronizers and arbiters, clock synchronization using PLL.
Design of ALU- a case study: data paths, adder, multiplier, shifter, power and speed trade-off in data path structures, power management.

TEXT BOOK:

1.J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, *Digital Integrated Circuits : A Design Perspective*, Second Edition, PH/Pearson.

REFERENCS:

1.S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits : Analysis and Design*, Third Edition, MH.
2.N. Weste, K. Eshraghian and M. J. S. Smith, *Principles of CMOS VLSI Design : A Systems Perspective*, Second Edition (Expanded), AW/Pearson.
3.J. P. Uyemura, *Introduction to VLSI Circuits and System*, Wiley.
4.R. J. Baker, H. W. Li and D. E. Boyce, *CMOS Circuit Design, Layout and Simulation*, PH.

EMBEDDED SYSTEMS LAB

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

(SVE537P)

LABORATORY EXPERIMENTS:

1. Comparison of transient response of dynamic NAND2 and dynamic NOT2 gates.
2. Design of Master Slave DFF.
3. Design and simulation of 8:1 MUX modeled in VHDL and VERILOG, and synthesis on FPGA.
4. Design and simulation of 8-bit synchronous counter with LOAD, RESET, and up/down controls, modeled in VHDL and VERILOG, and synthesis on FPGA.
5. Design and simulation of 8-bit parity checker/ generator modeled in VHDL and VERILOG, and synthesis on FPGA.
6. Design and simulation of 4-digit decade counter, modeled in VHDL and VERILOG, and synthesis on FPGA.
7. Design and simulation of 4-bit combinational multiplier, modeled in VHDL and VERILOG, and synthesis on FPGA.
8. Design and simulation of 4-bit sequential multiplier, modeled in VHDL and VERILOG, and synthesis on FPGA.
9. Design a serial port device that displays the last character written into the serial port on an LED matrix. Create a process that displays the character inputted from a keyboard. (*)
10. Design and simulation of 8-bit PISO and PIPO type registers modeled in VHDL and VERILOG, and synthesis on FPGA.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Real Time Systems
(SVE512T)

Real Time Computing: Introduction – issues in real time computing, structure of a real time system, task classes, performance measures for real time systems, estimating program run times-task assignment and scheduling – classical uni-processor scheduling algorithms – uni-processor scheduling tasks, task assignment, mode changes and fault tolerant scheduling.

Programming Languages and Tools: Programming languages and tools – desired language characteristics, data typing, control structures, facilitating hierarchical decomposition, packages, run – time (exception) error handling overloading and generics, multitasking, low level programming, task scheduling, timing specifications, programming environments, run – time support.

Real Time Databases: Real time databases – basic definition, real time vs general purpose databases, main memory databases, transaction priorities, transaction aborts, concurrency control issues, disk scheduling algorithms, two – phase approach to improve predictability, maintaining serialization consistency, databases for hard real time systems.

Communication: Real-time communication – communications medial, network topologies protocols, fault tolerant routing, fault tolerance techniques – fault types, fault detection, fault error containment redundancy data diversity, reversal checks, integrated failure handling.

Clock Synchronization: Introduction to clock synchronization – clock a non fault- tolerant synchronization algorithm, impact of faults, fault tolerant synchronization in hardware, fault tolerant synchronization in software.

Text Book:

1. Krishna C.M. Kang G, Shin, Real Time Systems, McGraw Hill.

REFERENCE:

1. Herma K, Real Time Systems – Design for distributed Embedded Applications

Kluwer Academic

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SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Hardware Software Co-Design
(SVE532T)

Co-Design Concepts: Problem description, goals of co-design, co-design steps, co-design approaches and accomplishments, challenges.

Architectures for Embedded Systems: Single processor-coprocessor architecture – multiprocessor architectures – internet protocol core based design – reconfigurable systems – platform-based design – interfacing embedded systems to the external environment: sensors.

System Modeling and Specification: Models of computation – finite state machines, extended finite state machines, control/data flow nets, petrinets, task graphs, hierarchical models – system specification languages – statecharts, very high speed integrated circuit hardware description language, system C.

Performance Modeling: System-level performance modeling vs. low-level performance modeling – modeling of execution speed (system latency) and energy consumption for hardware and software – estimation of memory requirements.

Hardware Synthesis: High-level synthesis – behavioral specification of hardware, module set allocation, resource binding, operation scheduling, controller synthesis.

TEXT BOOK:

Jean J. Labrosse, Embedded Systems Building Blocks: Complete and Ready-to-Use Modules in C, CMP Books.

REFERENCES

1. Arnold S. Berger, Embedded System Design CMP Books, USA.
2. Wayne Wolf, Computer as Components: Principles of Embedded Computer Systems Design, Morgan Kaufman Publishers.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Algorithms To Architectures
(SVE508T)

Complex Instruction Set Computers (CISC): Instruction Set, Characteristics and Functions, Addressing Modes, Instruction Formats, Architectural Overview, Processor Organization, Register Organization, Instruction Cycle, Instruction Pipelining, Pentium Processor, PowerPC Processor.

Reduced Instruction Set Computers (RISC): Instruction execution Characteristics, Register Organization, Reduced Instruction Set, Addressing Modes, Instruction Formats, Architectural Overview, RISC Pipelining, Motorola 88510, MIPS R4650, RISC Vs. CISC.

Pipeline Processing: Basic Concepts, Classification of Pipeline Processors, Instruction and Arithmetic Pipelining: Design of Pipelined Instruction Units, Pipelining Hazards and Scheduling, Principles of Designing Pipelined Processors.

Memory Architectures: Memory hierarchy design, Multiprocessors, thread level parallelism andmulti-core architectures, I/O buses. Arithmetic: Fixed point, Floating point and residue arithmetic, Multiply and Divide Algorithms.
Issues in arithmetic system design, Issues in the applications (optimizing the hardware – softwareinterface), ASIP, reconfigurable computing, Future microprocessor architectures.

Superscaler Processors: Overview, Design Issues, PowerPC, Pentium.

BOOKS:

1. Patterson, D.A. and Hennessy, J., Computer Architecture: A Quantitative Approach, Morgan Kaufmann.
2. Stallings, W., Computer Organization and Architecture: Designing for Performance, Prentice Hall.
3. Patterson, D.A. and Hennessy,J., Computer Organization and Design, Elsevier.
4. Flynn, M.J. and Oberman, S.F., Advanced Computer Arithmetic Design, Wiley.
5. Parhami, B., Computer Arithmetic Algorithms and Hardware Design, Oxford.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

WIRELESS SENSOR NETWORKS
(ECE205T)

Introduction, data acquisition, classification, sensor platforms, standards, applications, single-hop, multi-hop, design constraints, energy modeling, Distributed estimation, multi-sensor estimation, estimation theory for wireless sensor networks

Routing-challenges, flooding, gossip protocol, sensor protocol for information via negotiation, SPIN-EC, hierarchical routing, LEACH, PEGASIS, TEEN, geographic routing protocols-MECN, greedy forwarding, distance based blacklisting, PRR based routing, PRADA

Data aggregation techniques-energy efficiency, network lifetime, data accuracy, flat networks,hierarchical networks, cluster based networks, chain based data aggregation, power efficient data gathering protocol for sensor information systems, tree based data aggregation, energy aware data aggregation tree, grid based data aggregation, QoS aware protocols, trade-offs in data aggregation protocols-capacity-energy tradeoff

Localization: ranging techniques-received signal strength, time of arrival, time difference arrival, angle of arrival, range based localization protocols-, triangulation, multilateration, ad-hoc positioning system, range free localization-approximate point in triangualiton, introduction to security issues in WSNs

REFERENCES:

1. W. Dargie, C. Poellabauer, " Fundamentals of wireless sensor networks: Theory and practice",

2. I.F. Akyildiz, M.C. Vuran, " Wireless sensor networks",

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

RF Microelectronics
(SVE512T)

Active RF Components and **their characteristic parameters:**RF diodes, BJT, FET, HEMT.
RF Filter Design: Filter configurations, resonators, filter realizations – Butterworth, Chebychev.
High-Frequency Amplifier Design: Zeros as bandwidth enhancer, shunt series amplifier, bandwidth enhancement with f_T doublers, voltage references and biasing, tuned and cascaded amplifiers, RF Power Amplifier Design.
Noise in RF Circuits: types of noise, two port noise theory, Low-Noise Amplifier (LNA) – intrinsic MOSFET two port noise parameters, LNA topologies, design example, LNA Design example.
Phase-Locked Loops: PLL models, noise properties, sequential phase detectors, loop filters and charge pumps. **RF Oscillators**: tuned and negative resistance oscillators. **Mixers**: non-linear systems as mixers, multiplier based mixers.
RF amplifier design – a case study

TEXT BOOKS:

1. T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, CUP.
2. R. Ludwig and P. Bretchko, *RF Circuit Design*, Pearson.
3. B. Razavi, *RF Microelectronics*, PH.

REFERENCES:

1. B. Leung, *VLSI for Wireless Communication*, PH.
2. B. Razavi, *Phase-Locking in High-Performance Systems*, Wiley/IEEE.
3. B. Razavi, *Monolithic Phase-Locked Loops and Clock Recovery Circuits*, IEEE Press.
4. R. E. Best, *Phase-Locked Loops : Design, Simulation and Applications*, Fifth Edition, MH.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Mixed Signal IC Design
(SVE500T)

Data Converters: Introduction, Characteristic Parameters, Basic DAC and ADC Architectures.

Sampling and Aliasing, SPICE models for DACs and ADCs, Quantization Noise

Data Converter SNR: Clock Jitter, Improving SNR using Averaging, decimating filters for ADC's, Interpolating filters for DAC's, Band pass and high pass Sinc filters, using feedback to improve SNR.

Noise Shaping data converters: SPICE model, First order noise shaping, First order Noise Shaping, - Digital first order NS Modulators, Modulation Noise,Decimating and filtering the output of a NS Modulator,Analog Sync filter using SPICE,Analog Implementation of First order NS Modulator, Feedback DAC,Effect of parameters of Integrator, Forward modulator, op-amp. Second order Noise Shaping, Noise shaping Topologies.

Implementing data converters: R-2R topologies for DAC's – Current mode,voltage mode, wide swing current mode DAC, topologies without an op-amp,effects of op-amp parameters. Implementing ADC's- Implementing S/H,Cyclic ADC, Pipeline ADC-using 1.5 bits per stage, capacitor error averaging,comparator placement, clock generation, offsets and alternative topologies, Layout of Pipelined ADC's.

TEXT BOOK:

1. R. J. Baker, *CMOS Mixed Signal Cicuit Design*, Wiley/IEEE.

REFERENCE BOOKS:

1. A. Handkiewicz, *Mixed-Signal Systems : A Guide to CMOS Circuit Design*, Wiley-IEEE, 2002.
2. B. Razavi, *Principles of Data Conversion System Design*, IEEE Press.
3. P. V. A. Mohan, V. Ramachandran and M. N. S. Swamy, *Switched Capacitor Filters : Theory, Analysis and Design*, PH.
4. E. Sanchez-Sinencio and A. G. Andreou, *Low-Voltage/Low-Power Integrated Circuits and Systems : Low-Voltage Mixed-Signal Circuits*, IEEE.
5. Y. Tsividis, *Mixed Analog-Digital VLSI Devices and Technology*, MH.
6. S. Rabii and B. A. Wooley, *Design of Low-Voltage Low-Power Sigma-Delta Modulators*, Kluwer.
7. P. G. A. Jespers, *Integrated Converters : D-A and A-D Architectures, Analysis and Simulation*, OUP.
8. R. Van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters*, Kluwer.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Low Temperature Co-fired Ceramics Technology (SVE546T)

Introduction of Low Temperature co-fired ceramic technology. History, Advantages, Applications

Components: Hybrid Circuits, Inductors, Resistors, Transformers

LTCC technology, materials, LTCC process steps, bonding and packaging

Testing and Characterization of Technology, Reliability and residual stress issues

References:

1. Yoshihiko Imanaka “Low temperature co-fired ceramic technology”
2. Rodriguez, Antonio R & Arthur B.Wallace, “Ceramic capacitor and method of making it”, issued 10/10/1961
3. Stetson, Harold W., “Method of making multilayer circuits”, issued 06/22/1965
4. Roesler, Alexander W.: Schare, Joshua M: Glass, S.Jill; Ewsuk, Kevin G:Slama, George; Abel, David; Schofield, Daryl (June 2010), “Planar LTCC Transformers for High-Voltage Flyback Converters”, IEEE Transactions on Components and Packaging Technologies 33 (2): 359-372

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Computer Based Control Systems
(SVE514T)

Introduction: Block diagram of Digital Control System, Advantages & limitations of Digital Control System, comparison of continuous data & discrete data control system, Examples of digital control system.

Signal conversion and processing: Digital signal coding, data conversion and quantization, sampling period considerations, sampling as impulse modulation, sampled spectra & aliasing, Reconstruction of analog signals, zero order hold, first order hold, frequency domain characteristics, principles of discretization- impulse invariance, finite difference approximation of derivatives, rectangular rules for integration, Bilinear transformation, Mapping between s-plane & z-plane.

Representation of digital control system: Linear difference equations, pulse transfer function, input-output model, examples of first order continuous and discrete time systems, Signal flow graph applied to digital control systems.

Stability of digital control system in z-domain and Time domain analysis: Jury.s method, R.H. criteria, Comparison of time response of continuous data and digital control system, steady state analysis of digital control system, Effect of sampling period on transient response characteristics.

State space analysis: Discrete time state equations, significance of Eigen values & Eigen vectors, first and second companion form, Diagonalisation, Jordan Canonical form, similarity transformation, state transition matrix, solution of discrete time state equation, Discretization of continuous state space model & its solution. Liyapunov stability analysis, definitions, theorem, concept of equilibrium state.

Pole placement and observer designs: Concept of reachability, Controllability, Constructability & Observability, Design of controller via Pole placement method, state observer design, dead beat controller design, concept of duality.

TEXT BOOKS:

1. M. Gopal, "Digital Contol and State Variable Methods", Tata McGraw Hill.
2. K. Ogata, "Discrete Time Control Systems", Pearson Education Inc..
3. B.C. Kuo, "Digital Control Systems", Saunders College Publishing.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Low Power VLSI Design
(SVE510T)

Introduction: Power and Energy basics, Sources of power dissipation, important parameters for low power design, Low power design approaches.

Circuit level power optimizing techniques: Dynamic Power Optimization: multiple supply voltages, transistor sizing, technology mapping. Static power Optimization: Multiple thresholds, transistor stacking
Power saving efforts at architecture and algorithm levels, Reducing Interconnect power/energy, Power Distribution in Clock Distribution, Single driver vs. Distributed buffers, Buffer and device sizing, Zero skew vs. tolerant Skew, clock skew control and swing reduction. Energy Recovery CMOS.

Optimizing Power at Standby: Clock gating, power gating, body biasing, supply voltage ramping, Power reduction of memory in standby mode using voltage scaling and body biasing.

Optimizing Power at Runtime: Dynamic voltage and frequency scaling, adaptive body biasing, Power domains and power management.

Logic synthesis for low power: Low power design flow, power analysis methodology, Power estimation Techniques, Power Minimization Techniques.

Design of low power memory and arithmetic elements: memory architecture, SRAM cell metrics. power in cell array, Power for read and write access. Design of circuits for addition, Multiplication, Division.

Low power microprocessor Design – system power management, architectural trade-offs, choosing supply voltage, low power clocking, implementation options for low power.

TEXT BOOK:

1. J. M. Rabaey, M.Pedram, Low Power Design Methodologies, Kluwer-Academic Publn.

REFERENCES:

1. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, Digital Integrated Circuits : A Design Perspective, Second Edition, PH/Pearson.
2. K. Roy and S. C. Prasad, Low-Power CMOS VLSI Circuit Design, Wiley.
3. P. Chandrakasan and R. W. Broderson, Low-Power CMOS Design, IEEE Press.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Digital Signal Processing with FPGA
(SVE522T)

Overview of Digital Signal Processing (DSP) , Progrmmability and DSP, FPGA Technology , Classification by Granularity, Classification by Technology , FPGA and Programmable Signal Processors, Design Implementation , FPGA Structure , , Design with Intellectual Property Cores Challenges of FPGAs.

Adders, Multipliers, Dividers, Floating-Point Arithmetic Implementation, Multiply-Accumulator (MAC) and Sum of Product (SOP), Computation of Special Functions Using CORDIC, Computation of Special Functions using MAC Calls,

Designing FIR Filters: Constant Coefficient FIR Design, Infinite Impulse Response (IIR) Digital Filters: IIR Coefficient Computation, IIR Filter Implementation, Fast IIR Filter

Multirate Signal Processing: Decimation and Interpolation, Poly-phase Decomposition, Multistage Decimator , Frequency-Sampling Filters as Band pass Decimators , Design of Arbitrary Sampling Rate Converters , Filter Banks, Wavelets

The Discrete Fourier Transform Algorithms, The Fast Fourier Transform(FFT)Algorithms, Cryptography Algorithms for FPGAs, FPGA Design of the LMS Algorithm, RTL to GDS flow case studies.

REFERENCES:

1. Digital Signal Processing with Field Programmable Gate Arrays **Uwe Meyer-Baese , S**pringer.
2. FPGA-based Implementation of Signal Processing Systems. by Roger Woods, John Mcallister, WILEY
3. VLSI Digital Signal Processing Systems: Design and implementation by Keshab K. Parhi, WILEY
4. VLSI Synthesis of DSP Kernels: Algorithmic and Architectural Transformationsby Mahesh Mehendale, Sunil D. Sherlekar, Kluwer Academic Publisher

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

Embedded Microcontroller & Applications
(SVE524T)

AVR microcontroller architecture:Developers Guide Designing and Optimizing System Software, Elsevier 2007. 5. ARM Architecture Reference Manual 6. LPC213x User Manual – instruction set – programming techniques –Assembly language & C programming- Development Tools – Cross Compilers – Hardware Design Issues .

Peripheral of AVR microcontroller:I/O Memory – EEPROM – I/O Ports –SRAM –Timer –UART – Interrupt Structure- Serial Communication with PC – ADC/DAC Interfacing .

ARM architecture and programming;Arcon RISC Machine – Architectural Inheritance – Core & Architectures -Registers – Pipeline - Interrupts – ARM organization - ARM processor family – Co-processors. Instruction set – Thumb instruction set – Instruction cycle timings - The ARM Programmers model – ARM Development tools – ARM Assembly Language Programming and C compiler programming.

ARM application development : Introduction to DSP on ARM –FIR Filter – IIR Filter – Discrete fourier transform – Exception Handling – Interrupts – Interrupt handling schemes- Firmware and bootloader – Example: Standalone - Embedded Operating Systems – Fundamental Components - Example Simple little Operating System

Design with ARM microcontrollers: Integrated development environment – Standard I/O Libraries - User Peripheral Devices – Application of ARM processor: Wireless Sensor Networks, Robotics.

REFERENCES:

1. Steve Furber, „ARM system on chip architecture, Addison Wesley.

2. Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield ARM System

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (Embedded Systems)

DESIGN LAB
(SVE536P)

NOTE: The experiments to be decided by the teacher and need not be same in all the semesters.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Scheme for M.Tech (VLSI Design)

First Semester

Sl. No.	Course No.	Subject	L-T-P	Credits
1	**SVE501T**	Digital IC Design	3-0-0	3
2	**SVE503T**	Analog IC Design	3-0-0	3
3	**SVE505T**	Hardware Description Languages and FPGA based Design	3-0-0	3
4		Elective-1	3-0-0	3
5		Elective-2	3-0-0	3
6	**SVE507P**	VLSI Design Lab-I	0-0-4	2
7	**SVE509P**	Seminar	0-0-2	1

Total Credits = 18

Semester-I: Electives

	Elective-1
1	Embedded System Fundamentals **(SVE511T)**
2	DSP and ASIP Architectures **(SVE513T)**
3	Introduction to MEMs **(SVE515T)**
	Elective-2
1	Nano Technology **(SVE517T)**
2	Hardware Algorithms For Computer Arithmetic (**SVE519T)**
3	Memory Design and Testing **(SVE521T)**

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Second Semester

Sl. No.	Course No.	Subject	L-T-P	Credits
1	**SVE500T**	Mixed Signal IC Design	3-0-0	3
2	**SVE502T**	Modeling of Semiconductor Devices	3-0-0	3
3		Elective-1	3-0-0	3
4		Elective-2	3-0-0	3
5		Elective-3	3-0-0	3
6	**SVE504P**	VLSI Design Lab-II	0-0-4	2
7	**SVE506P**	Seminar	0-0-2	1

Total Credits = 18

Semester-II: Electives

	Elective-1
1	Integrated Electronic System Design (**SVE508T)**
2	Low-Power VLSI Design (**SVE510T)**
3	Real Time Systems (**SVE512T)**
	Elective-2
1	RF Micro-electronics (**SVE514T)**
2	Advance Digital Signal Processing **(SVE516T)**
3	Multimedia Systems **(SVE518T)**
	Elective-3
1	VLSI Testing And Verification **(SVE520T)**
2	Digital Signal Processing with FPGAs **(SVE522T)**
3	CDMA Systems **(SVE524T)**

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Third Semester

Sl. No.	Course No.	Subject	L-T-P	Credits
1	**SVE601P**	Preparatory Work for Dissertation	0-0-20	10

Total Credits = 10

NOTE-I: (**Semester-III).**

The Preparatory Work for Dissertation shall be evaluated by a committee comprising the following [on the basis of one mid semester seminar and one end semester seminar presented and one end semester report submitted by the candidate].

1) HOD or faculty nominee proposed by HOD.
2) Dissertation Supervisor (and co-supervisor)
3) Two senior most faculty members of the department.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Fourth Semester

Sl. No.	Course No.	Subject	L-T-P	Credits
1	SVE602P	Dissertation	0-0-32	16

Total Credits = 16

NOTE-II: (Semester – IV)

(i) The Dissertation shall be evaluated by a committee comprising the following through a presentation cum viva-voce examination.
   1) HOD or faculty nominee proposed by HOD.
   2) Dissertation Supervisor (and co-supervisor)
   3) One external expert appointed by the Department

(ii) For award of grade, following criteria to be used.

Grade Awarded	Conditions to be fulfilled
A+	One paper accepted/published in SCI Journal
A	One good quality paper accepted/published in non-paid journal or two good quality papers presented in international / national conference.*
B	One good quality paper presented in international conference
C/D	In other cases

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Digital IC Design
(SVE501T)

Modeling of Interconnects: Interconnect parameters, wire models, SPICE models for wires. **CMOS Inverter:** Static and Dynamic Behavior, Power, Energy and Energy Delay, Technology scaling and its impact.

Design of CMOS Combinational Logic Gates: Static and dynamic CMOS Design, Speed and power dissipation in dynamic circuits, cascading of gates, designing logic for reduced supply voltages, simulation of logic circuits.

Design of CMOS Sequential Logic Circuits: Static and dynamic latches and registers, alternative register styles, pipelined sequential circuits, non-bistable sequential circuits.

Custom, Semi-custom, and Structured array design approaches: Cell Based Design – standard, compiled , macro cells, mega cells, ArrayBased Design – mask programmable and rewired arrays.

Coupling with Interconnects: Effects of Interconnect Parasitics, Advanced Interconnect techniques.

Timing issues in Digital Circuits: Timing classification, synchronous timing basics, sources of skew and jitter, clock distribution techniques, latch-based clocking, Self-timed circuit design, synchronizers and arbiters, clock synchronization using PLL.

Design of ALU- a case study: data paths, adder, multiplier, shifter, power and speed trade-off in data path structures, power management.

TEXT BOOK:

1. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, *Digital Integrated Circuits : A Design Perspective*, Second Edition, PH/Pearson.

REFERENCES:

1. S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits : Analysis and Design*, Third Edition, MH.
2. N. Weste, K. Eshraghian and M. J. S. Smith, *Principles of CMOS VLSI Design : A Systems Perspective*, Second Edition (Expanded), AW/Pearson.
3. J. P. Uyemura, *Introduction to VLSI Circuits and System*, Wiley.
4. R. J. Baker, H. W. Li and D. E. Boyce, *CMOS Circuit Design, Layout and Simulation*, PH.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Analog IC Design
(SVE503T)

Integrated CMOS Amplifiers: Why integrated CMOS, single stage amplifiers-common source amplifiers with different types of loads, source follower, common gate amplifiers, cascade stage, choice of device models, Differential amplifiers-analysis of single ended and differential output amplifiers, common mode response, differential pair with MOS load, gilbert cells.
Comparators.
Current Mirrors: Basic current mirriors, cascade current mirriors, analysis of current mirrors, **Frequency response of amplifiers**: general considerations, frequency response of different types of amplifiers, **Sources of Noise in CMOS Amplifiers:** types of noise**,** representation of noise, noise in amplifiers.
CMOS Band gap References: supply independent biasing, temperature independent references, PTAT current generation , constant G_m biasing , speed and noise issues,
Feedback in Amplifiers: feedback topologies, effect of loading, effect of feedback on noise, **CMOS Operational Amplifiers-** performance parameters, one-stage and two-stage Op Amps, gain boosting, input range limitations, slew rate.
CMOS Phase Lacked Loops: simple PLLs, charge pump PLLs, non ideal effects in PLLs, applications in frequency multiplication, skew and jitter reduction.

TEXT BOOK:

1. B. Razavi, *Design of Analog CMOS Integrated Circuits*, MH.

REFERENCES:

1. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Second Edition, OUP.
2. R. Gregorian, *Introduction to CMOS Op-Amps and Comparators*, Wiley.
3. K. R. Laker and W. M. C. Sansen, *Design of Analog ICs and Systems*, MH.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Hardware Description Languages and FPGA Based Design
(SVE505T)

Verilog : basic concepts- Lexical conventions, data types, system tasks and compiler directives. Modules and ports. Gate level modeling- gate types, various types of gate delay specifications. Data flow modeling- assignments, delays, expressions, operators, . Behavioral modeling- structured procedures, procedural assignments, timing controls, conditional statements, loops, sequential and parallel blocks, generate blocks. Tasks and functions

FPGA Architectures and Technology. Historical background, channel type FPGA- Xilinx 3000 and Actel ACT2 family, structured programmable array logic, programming FPGAs, benchmarking of FPGAs. Recent developments- new architectures such as Altera FLEX, Pilkington (Motorola/ Toshiba), Xilinix XC4000, field programmable interconnect.

VHDL Synthesis for FPGA Implementation.: Mapping of statements to gate-assignment statements, logical, arithmetic and relational operators, vectors and slices, IF, Process, Case, Loop, Null, Wait statements. Modeling of flip-flops and latches. Modeling of FSM for synthesis. Some examples of synthesizable constructs.

Verilog Synthesis for FPGA Implementation: Verilog constructs and operators, interpretation of Verilog constructs, synthesis design flow- RTL to gates, translation, un-optimized intermediate representations, logic optimization, technology mapping and optimization, technology library, design constraints, optimized gate level description.

TEXT BOOKS:

1 S. Palnitkar, *Verilog HDL : A Guide to Digital Design and Synthesis*, PH/Pearson.
2 K. Coffman, *Real World FPGA Design with Verilog*, PH.

REFERENCES:

1. P.J. Ashenden, *The Designer's Guide to VHDL*, Second Edition, Morgan Kaufmann.
2. C. H. Roth, *Digital System Design with VHDL*, PWS/Brookscole.
3. R. C. Seals and G. F. Whapshott, *Programmable Logic : PLDs and FPGAs*, MH.
4. A,K. Sharma, *Programmable Logic Handbook : PLDs, CPLDs and FPGAs*, MH.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Embedded System Fundamentals

(SVE511T)

An Introduction to Embedded Systems : An Embedded System, Processor in the System, Other Hardware Units, and Software Embedded into a System, Exemplary Embedded Systems, Embedded System – On- Chip (SOC) and in VLSI Circuit.

Processor and Memory Organization: Structural Units in a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded Systems, Allocation of Memory to Program Cache and Memory Management Links, Segments and Blocks and Memory Map of a System, DMA, Interfacing Processors, Memories and Input Output Devices.

Devices and Buses for Device Networks: I/O Devices, Timer and Counting Devices, Serial Communication Using the "1^2C" (Inter IC) CAN (controller area network), Profibus Foundation Field Bus and Advanced I/O Buses Between the Network Multiple Devices. Host Systems or Computer Parallel Communication between the Networked I/O Multiple Devices using the ISA, PCI, PCI-X and Advanced Buses.

Device Drivers and Interrupts Servicing Mechanics: Device Drivers, Parallel Port and Serial Prot Device Drives in a System, Device Drovers for Internal Programmable Timing Devices, Interrupt Servicing Mechanism.

Programming Concepts and Embedded Programming in C, C++, VC++ and JAVA: Interprocess Communication and Synchronization of Processes, Task and Threads, Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Interprocess Communication.

Hardware-Software Co-design in an Embedded System: Embedded System Project Management Embedded System Design and Co-Design issues in System Development Process.

Design Cycle in the Development Phase for an Embedded System: Use of Target Systems, Use of Software Tools for Development of an Embedded System, Use of Scopes and Logic Analysis for System, Hardware Tests, Issues in Embedded System Design.

Text Books:

Raj Kamal, "Embedded Systems: Architecture, Programming and Design", TMH.

David Simon, "An Embedded Software Primer", Pearson Education.

Reference:

Arnold S Burger, "Embedded System Design", CMP Steve Heath; Butterworth Heinenann, "Embedded System Design: Real World Design," Netwon Mass USA.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

DSP and ASIP Architectures
(SVE513T)

Implementations of Basic DSP Operations -Adders, Multipliers, Dividers; Discrete Fourier Transform Implementation-characteristics of DFT- direct implementation of DFT, fast fourier transforms; Fixed-Point versus Floating-Point Operations; Pipelining and Parallelism; Re-timing, **Unfolding-** algorithm, properties and applications of unfolding, **Folding**- folding transformation, register minimization in folded architectures, folding of multirate systems..

Systolic/Array Architectures-implementation of array processors, algorithmic representations, **Mapping methods**-mapping without changing the number of nodes and with reduced number of nodes, projection method, multiprojection, partitioning, projection of nodes with different operations; **Programmable DSP Architectures**-the architecture of standard computer, architectural approaches for DSP processors, characteristics of available DSPs, FIR filter program, DFT program, instruction pipelining, special arithmetic modules, on-chip memory; Memory Structures and Addressing.

Implementation of FIR- signal flow graph of 1-D FIR filter, implementation for low throughput and for high throughput, 2-D FIR filters, decimation filters, interpolation filters, filter banks. Implementation of IIR Filter Structures-recursive filters in direct form, MSB first arithmetic, lookahead techniques.

ASIP Related Terms; Power/Energy/Performance Issues; ASIP Design Space; ASIP Design Flow; Hardware-Software Boundary and Trade-offs; Case Studies.

TEXT BOOKS:

1. P. Lapsley, J. Bier, A. Shoham and E. A. Lee, *DSP Processor Fundamentals : Architectures and Features*, Wiley/IEEE.
2. P. Pirsch, *Architectures for Digital Signal Processing*, Wiley.
3. T. Glokler and H. Meyr, *Design of Energy-Efficient Application Specific Instruction Set Processors*, Kluwe.

REFERENCES:

1. K. K. Parhi, *VLSI Digital Signal Processing Systems : Design and Implementation*, Wiley.
2. V. K. Madisetti, *VLSI Digital Signal Processors*, Butterworth-Heinemann/IEEE Press.
3. A. Bateman and I. Paterson-Stephens, *The DSP Handbook*, PH/Pearson.
4. S. M. Kuo, *Digital Signal Processors : Architectures, Implementations and Applications*, PH/Pearson.
5. L. Wanhammar, *DSP Integrated Circuits*, AP.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Introduction To MEMS

(SVE515T)

Introduction, Basic Structures of MEM Devices: (Canti Levers, Fixed Beams diaphragms).Broad Response of Micro Electromechanical Systems (MEMs) to Mechanical (force, pressure etc.) Thermal, Electrical, Optical and Magnetic Stimuli, Compatibility of MEMS from the point of Power Dissipation, Leakage etc.

Review of Mechanical Concepts: Stress, Strain, Bending Moment, Deflection Curve. Differential Equations Describing the Deflection under Concentrated Force, Distributed Force, Deflection Curves for Canti Levers – Fixed Beam. Electrostatic Excitation – Columbic Force between the Fixed and Moving Electrodes. Deflection with Voltage in C.L, Deflection Vs Voltage Curve, Critical Fringe Fields – Field Calculations using Laplace Equation. Discussion on the Approximate Solutions - Transient Response of the MEMS.

Two Terminal MEMS: Capacitance Vs Voltage Curve – Variable Capacitor. Applications of Variable Capacitors. Two Terminal MEM Structures.Three Terminal MEM Structures – Controlled Variable Capacitors – MEM as a Switch and Possible Applications.

MEM Circuits & Structures for Simple Gates: AND, OR, NANO, NOR , Exclusive OR, simple MEM Configurations for Flip-Flops Triggering, Applications to Counters, Converse Applications for Analog Circuits like Frequency Converters, Wave Shaping. RF Switches for Modulation. MEM Transducers for Pressure, Force Temperature.Optical MEMS.

MEM Technologies: Silicon Based MEMS- Process Flow- Brief Account of Various Processes and Layers like Fixed Layer, Moving Layers, Spacers Etc. Etching Technologies. Metal Based MEMS: Thin and Thick Film Technologies for MEMS. PROCESS flow and Description of the Processes.Status of MEMS in the Current Electronics scenario.

BOOKS:

1. Gabriel M.Review, “R.F. MEMS Theory, Design and Technology”, John Wiley & Sons.
2. ThimoShenko, “Strength of Materials”, CBS Publishers & Distributors.
3. Ristic L.(Ed.), “Sensor Technology and Devices”, Artech House, London.
4. ServeyE.Lyshevski, “MEMS and NEMS, Systems Devices; and Structures”, CRC Pres.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Nano-Technology
(SVE517T)

Introduction to nanoscale systems. Length, energy, and time scales

Top-down approach to nanolithography, Spatial resolution of optical, deep-ultraviolet, x-ray, electron beam, and ion beam lithography.

Single electron transistors, coulomb blockade effects in ultra-small metallic tunnel junctions.

Quantum confinement of electrons in semiconductor nanostructures: two-dimensional confinement (quantum wells). Band gap engineering. Eptaxy.

Landauer-Buttiker formalism for conduction in confined geometries.

One dimensional confinement: Quangum point contacts, quantum dots.

Bottom-up approach. Chemical self-assembly, carbon nanotubes.

Molecular electronics. Self-assembled monolayers. Electrochemical techniques; applications in biological and chemical detection.

Atomic scale characterization techniques: scanning tunneling microscopy, atomic force microscopy.

Introduction to quantum methods of information processing.

BOOKS:

1. David Ferry, Transport in Nanostructures, Cambridge University Press.
2. Y. Imry, Introduction to Mesoscopic Physics, Oxform university Press.
3. S. Datta, Electron Transport in Mesoscopic Systems, Cambridge University Press.
4. H. Grabert and M. Devoret, Single Charge Tunneling, Plenum Press.
5. Beenaker and Van Houten, Quantum Transport in Semiconductor Nanostructures, in Solid State Physics v. 44, eds. Ehernreich and Turnbull, Academic Press, 1991. P. Rai-Choudhury, Handbook of Microlithography, Micromachining & Microfabrication, SPIE.
6. B. Venkataramani and M. Bhaskar, *Digital Signal Processors : Architecture, Programming and Applications*, TMH.
7. E. E. Swartzlander, *Application Specific Processors*, Kluwer, 1997. Meyer-Baese, *DSP with FPGAs*, Springer-Verlag.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Hardware Algorithms For Computer Arithmetic

(SVE519T)

Review of Number systems, their encoding and basic arithmetic operations, Class of Fixed-Radix Number Systems, Unconventional fixed-point number systems, Representing Signed Numbers, Negative-radix number Systems, Redundant Number Systems, Residue Number Systems.

Manchester carry chains and adders, Carry-Look-ahead Adders, Carry determination as prefix computation, Alternative parallel prefix networks, VLSI implementation aspects, Variations in Fast Adders, Simple carry-skip and Carry-select adders, Hybrid adder designs, Optimizations in fast adders, Multi-Operand Addition, Wallace and Dadda trees, Parallel counters, Generalized parallel
counters, Adding multiple signed numbers.

Shift/add multiplication algorithms, Programmed multiplication, Basic hardware multipliers, Multiplication of signed numbers, Multiplication by constants, Preview of fast multipliers, High-Radix Multipliers, Modified Booth's recoding, Tree and Array Multipliers, Variations in Multipliers,

Shift/subtract division algorithms, Programmed division, Restoring hardware dividers, Non-restoring and signed division, Division by constants, Preview of fast dividers, High-Radix Dividers, Variations in Dividers, Combined multiply/divide units, Hardware implementation.

Floating-point arithmetic operations, Rounding schemes, Logarithmic number systems, Floating-point adders, Barrel-shifter design, Leading-zeros/ones counting, Floating-point multipliers, Floating-point dividers, Arithmetic Errors and Error Control.

Square-Rooting Methods, The CORDIC Algorithms, Computinglogarithms, Exponentiation, Approximating functions, Merged arithmetic, Arithmetic by Table Lookup, Tradeoffs in cost, speed, and accuracy.

BOOKS:

1. Parhami, B., Computer Arithmetic: Algorithms and Hardware Design, Oxford University Press.
2. Koren, I., Computer Arithmetic Algorithms, 2nd Edition, Uni Press.
3. Ercegovac, M. and Lang, T., Digital Arithmetic, Elsevier.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Memory Design and Testing
(SVE521T)

Introduction to Semiconductor Memories and Technologies: Internal organization of memory chips, basic memory elements, memory types, trends in SRAM and DRAM design, Non-volatile memory technologies.

SRAM and DRAM Cell Design; basic structures-NMOS static/dynamic circuits, CMOS circuits, cell design.

Cache Memory Design.: concept of locality in space and time, interfacing cache memory with CPU, associated problems-parasitic capacitances, critical timing paths, bus turnaround.

Memory Testing: Reliability-failure mechanisms for memories, reliability modeling and fault detection, Yield, Radiation Effects-radiation types effecting the memory, radiation hardening techniques

TEXT BOOKS:

1. K. Itoh, *VLSI Memory Chip Design*, Springer-Verlag.
2. B. Keeth and R. J. Baker, *DRAM Circuit Design : A Tutorial*, Wiley/IEEE.

REFERENCES:

1. B. Prince, *Semiconductor Memories : A Handbook of Design, Manufacture and Application*, Second Edition, Wiley.
2. B. Prince, *High Performance Memories*, Wiley.
3. B. Prince, *Emerging Memories : Technologies and Trends*, Kluwer.
4. A. K. Sharma, *Advanced Semiconductor Memories : Architectures, Designs and Applications*, Wiley/IEEE.
5. T. P. Haraszti, *CMOS Memory Circuits*, Kluwer.
6. J. Handy, *The Cache Memory Book*, Second Edition, AP.
7. M. I. Elmasry, *Digital MOS Circuits II : with Applications to Processors and Memory Design*, IEEE Press.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

VLSI Design Lab-I
(SVE507P)

Laboratory Experiments:

1. Design and simulation of 8-bit SISO and SIPO type registers modeled in VHDL and VERILOG, and synthesis on FPGA.
2. Circuit simulation of CMOS Inverter-study of static and dynamic behavior.
3. Study of the effect of variation in V_{DD} and Temperature on static and dynamic behavior of CMOS Inverter.
4. Design and simulation of 8:1 MUX modeled in VHDL and VERILOG, and synthesis on FPGA.
5. Comparison of transient response of dynamic NAND2 and dynamic NOR2 gates.
6. Design and simulation of 8-bit parity checker/generator modeled in VHDL and VERILOG, and synthesis on FPGA.
7. Design and simulation of 4-bit combinational multiplier, modeled in VHDL and VERILOG, and synthesis on FPGA.
8. Design and simulation of 4-bit sequential multiplier, modeled in VHDL and VERILOG, and synthesis on FPGA.
9. Design and simulation of CS, CG and CD amplifier.
10. Design and simulation of a single stage CMOS operational amplifier.
11. Layout design and simulation of a differential amplifier.
12. Design and simulation of positive TC and negative TC band gap reference.
13. Layout design and simulation of positive TC band gap reference.
14. Design and simulation of a second order switched capacitor filter.
15. Design and simulation of simple phase locked loop.
16. Design and simulation of charge pump phase locked loop.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Mixed-Signal IC Design
(SVE500T)

Data Converters: Introduction, Characteristic Parameters, Basic DAC and ADC Architectures.

Sampling and Aliasing, SPICE models for DACs and ADCs, Quantization Noise

Data Converter SNR: Clock Jitter, Improving SNR using Averaging, decimating filters for ADC's, Interpolating filters for DAC's, Band pass and high pass Sinc filters, using feedback to improve SNR.

Noise Shaping data converters: SPICE model, First order noise shaping, First order Noise Shaping, - Digital first order NS Modulators, Modulation Noise,Decimating and filtering the output of a NS Modulator,Analog Sync filter using SPICE,Analog Implementation of First order NS Modulator, Feedback DAC,Effect of parameters of Integrator, Forward modulator, op-amp. Second order Noise Shaping, Noise shaping Topologies.

Implementing data converters: R-2R topologies for DAC's – Current mode,voltage mode, wide swing current mode DAC, topologies without an op-amp,effects of op-amp parameters. Implementing ADC's- Implementing S/H,Cyclic ADC, Pipeline ADC-using 1.5 bits per stage, capacitor error averaging,comparator placement, clock generation, offsets and alternative topologies, Layout of Pipelined ADC's.

TEXT BOOK:

1. R. J. Baker, *CMOS Mixed Signal Cicuit Design*, Wiley/IEEE, 2002.

REFERENCE BOOKS:

1. Handkiewicz, *Mixed-Signal Systems : A Guide to CMOS Circuit Design*, Wiley-IEEE, 2002.
2. Razavi, *Principles of Data Conversion System Design*, IEEE Press, 1995.
3. P. V. A. Mohan, V. Ramachandran and M. N. S. Swamy, *Switched Capacitor Filters : Theory, Analysis and Design*, PH, 1995.
4. E. Sanchez-Sinencio and A. G. Andreou, *Low-Voltage/Low-Power Integrated Circuits and Systems : Low-Voltage Mixed-Signal Circuits*, IEEE, 1999.
5. Y. Tsividis, *Mixed Analog-Digital VLSI Devices and Technology*, MH, 1996.
6. S. Rabii and B. A. Wooley, *Design of Low-Voltage Low-Power Sigma-Delta Modulators*, Kluwer, 1998.
7. P. G. A. Jespers, *Integrated Converters : D-A and A-D Architectures, Analysis and Simulation*, OUP, 2001.
8. R. Van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters*, Kluwer, 1994.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Modeling of Semiconductor Devices
(SVE502T)

Brief review of silicon devices & fabrication processes, Recent developments in microelectronic devices.

p-n junction- current flow mechanisms , DC , small signal, transient model under forward and reverse bias conditions, circuit models for different types of p-n junction diodes.

Bipolar junction transistor-current flow in BJT's, charge control models for BJT's, DC and small signal equivalent circuits, Gummel Poon mode, MEXTRAM model, HICUM model, second order effects- effects of non-uniform doping in the base, high injection, heavy doping effects in emitter, emitter crowding , non conventional BJT's- poly silicon emitter transistor, HBT.

MOSFETs: modeling of weak and strong inversion in three terminal and four terminal MOS transistors, effect of small dimensions- DIBL, charge sharing, channel length modulation, hot carrier effects. Small signal models of MOSFETs for low and medium frequencies, large signal modeling of MOS transistor in dynamic operation. Level 1, 2, 3, 4(BSIM) models ,HSPICE Level 50 model.

Modeling for circuit simulation: types of models combining several effects into one physical model, parameter extraction, properties of good models

TEXT BOOKS:

1. N. Dasgupta and A. Dasgupta, *Semiconductor Devices: Modeling and Technology*, PHI .
2. Y.Tsividis, *Operation and Modeling of The MOS Transistor*, OUP .

REFERENCE BOOKS:

3. M. S. Tyagi, *Introduction to Semiconductor Materials and Devices*, Wiley.
4. M. Shur, *Physics of Semiconductor Devices*, PH.
5. D. Forty, *MOSFET Modeling with SPICE : Principles and Practices*, PH.
6. B. G. Streetman, *Solid State Electronic Devices*, Fourth Edition, PH.
7. R. Raghuram, *Computer Simulation for Electronic Circuits*, Wiley.
8. W. Liu, *MOSFET Models for SPICE Including BSIM3v3 and BSIM4*, Wiley.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Integrated Electronic System Design
(SVE508T)

Introduction: Electronic Systems; Sensors and Actuators; Microcomputers and Micro-controllers.

Packaging of Digital Systems: ICs – chip wiring, wire bonds and solder balls, package types ,multi chip modules. PCBs – construction, electrical properties, dimensional constraints. Chassis and Cabinets –Back-planes and Motherboards, Wires, Cables and Connectors.

Noise in Digital Systems: Power Supply Noise, Cross Talk, Inter symbol interference, EMI and other noise sources, managing noise budget. **Clocking and Timing Issues:** Skew and Jitter Analysis, Properties of delay/combinational/storage elements, open loop and closed loop timing, clock distribution.

Bus-based System Design: Bus Buffers, Bus Clock, Data Transfer Rate, Bus Protocols.

System Design Using i8051 Micro-controller (or 68HC12 Micro-controller): Design of a temperature control system..

Real-time System Design Issues.

TEXT BOOKS:

1. W. J. Dally and J. W. Poulton, *Digital Systems Engineering*, CUP,.
2. N. Storey, *Electronics : A Systems Approach*, AW/Pearson,.
3. S. D. Burd, *Systems Architecture*, Thomson,.

REFERENCES:

1. G. Lipovski, *Introduction to Micro-controllers (MC 68HC12),* AP,.
2. G. Lipovski, *Single and Multi-Chip Micro-controller Interfacing (MC 68HC12),* AP.
3. F. M. Cady, *Microcontrollers and Microcomputers : Principles of Software and Hardware Engineering*, OUP.
4. *M. Predko,* Handbook of Microcontrollers, *MH.*

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Low-Power VLSI Design
(SVE510T)

Introduction:Power and Energy basics, Sources of power dissipation, important parameters for low power design, Low power design approaches.

Circuit level power optimizing techniquies: Dynamic Power Optimization: multiple supply voltages, transistor sizing, technology mapping. Static power Optimization:Multiple thresholds, transistor stacking
Power saving efforts at architecture and algorithm levels, Reducing Interconnect power/energy, Power Distribution in Clock Distribution, Single driver vs. Distributed buffers, Buffer and device sizing, Zero skew vs. tolerant Skew, clock skew control and swing reduction. Energy Recovery CMOS.

Optimizing Power at Standby: Clock gating, power gating, body biasing, supply voltage ramping, Power reduction of memory in standby mode using voltage scaling and body biasing.

Optimizing Power at Runtime: Dynamic voltage and frequency scaling, adaptive body biasing, Power domains and power management.

Logic synthesis for low power: Low power design flow, power analysis methodology, Power estimation Techniques, Power Minimization Techniques.

Design of low power memory and arithmetic elements: memory architecture,SRAM cell metrics.power in cell array, Power for read and write access.Design of circuits for addition, Multiplication, Division.

Low power microprocessor Design – system power management, architectural trade-offs, choosing supply voltage, low power clocking, implementation options for low power.

TEXT BOOK:

1. J. M. Rabaey, M.Pedram, Low Power Design Methodologies, Kluwer-Academic Publn.

REFERENCES:

1. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, Digital Integrated Circuits : A DesignPerspective, Second Edition, PH/Pearson.
2. K. Roy and S. C. Prasad, Low-Power CMOS VLSI Circuit Design, Wiley.
3. P. Chandrakasan and R. W. Brodersen, Low Power Digital CMOS Design, Kluwer.
4. P. Chandrakasan and R. W. Broderson, Low-Power CMOS Design, IEEE Press.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Real Time Systems
(SVE512T)

Real Time Computing: Introduction – issues in real time computing, structure of a real time system, task classes, performance measures for real time systems, estimating program run times-task assignment and scheduling – classical uniprocessor scheduling algorithms – uniprocessor scheduling tasks, task assignment, mode changes and fault tolerant scheduling.

Programming Languages and Tools: Programming languages and tools – desired language characteristics, data typing, control structures, facilitating hierarchical decomposition, packages, run – time (exception) error handling overloading and generics, multitasking, low level programming, task scheduling, timing specifications, programming environments, run – time support.

Real Time Databases: Real time databases – basic definition, real time vs general purpose databases, main memory databases, transaction priorities, transaction aborts, concurrency control issues, disk scheduling algorithms, two – phase approach to improve predictability, maintaining serialization consistency, databases for hard real time systems.

Communication: Real-time communication – communications medial, network topologies protocols, fault tolerant routing, fault tolerance techniques – fault types, fault detection, fault error containment redundancy data diversity, reversal checks, integrated failure handling.

Clock Synchronization: Introduction to clock synchronization – clock a non fault- tolerant synchronization algorithm, impact of faults, fault tolerant synchronization in hardware, fault tolerant synchronization in software.

TEXT BOOK:

Krishna C.M. Kang G, Shin, Real Time Systems, McGraw Hill.

REFERENCE:

Herma K, Real Time Systems – Design for distributed Embedded Applications

Kluwer Academic.

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SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

RF Microelectronics
(SVE514T)

Active RF Components and their characteristic parameters:RF diodes, BJT, FET, HEMT.

RF Filter Design: Filter configurations, resonators, filter realizations – Butterworth, Chebychev.

High-Frequency Amplifier Design: Zeros as bandwidth enhancer, shunt series amplifier, bandwidth enhancement with f_T doublers, voltage references and biasing, tuned and cascaded amplifiers, RF Power Amplifier Design.

Noise in RF Circuits: types of noise, two port noise theory, Low-Noise Amplifier (LNA) – intrinsic MOSFET two port noise parameters, LNA topologies, design example, LNA Design example.

Phase-Locked Loops: PLL models, noise properties, sequential phase detectors, loop filters and charge pumps. **RF Oscillators**: tuned and negative resistance oscillators. **Mixers**: non-linear systems as mixers, multiplier based mixers.

TEXT BOOKS:

1. T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, CUP.
2. R. Ludwig and P. Bretchko, *RF Circuit Design*, Pearson.
3. B. Razavi, *RF Microelectronics*, PH.

REFERENCE BOOKS:

1. B. Leung, *VLSI for Wireless Communication*, PH.
2. B. Razavi, *Phase-Locking in High-Performance Systems*, Wiley/IEEE.
3. B. Razavi, *Monolithic Phase-Locked Loops and Clock Recovery Circuits*, IEEE Press.
   R. E. Best, *Phase-Locked Loops : Design, Simulation and Applications*, Fifth Edition, MH.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Advance Digital Signal Processing
(SVE522T)

Decimation, Interpolation, Implementation of sampling rate converters, applications of sampling rate converters, polyphase structures, two-channel and M-channel filter banks.

Innovations representations of stationary random processes, linear prediction, linear prediction filters, Wiener filters, Kalman filters.

Applications of adaptive filters, adaptive direct form filters, LMS and RLS algorithms, adaptive lattice ladder filters.

Spectrum estimation from finite duration observations, parametric and nonparametric power spectrum estimation methods, filter bank methods, eigenanalysis algorithms.

TEXT BOOK

1. J.G. Proakis and D. Manolakis Digital signal processing PHI

REFERENCE BOOKS

1. P.P. Vaidyanathan Multirate filter banks PHI/Pearson.
2. Simon Haykin Adaptive filter Theory PHI/Pearson.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Multimedia Systems
(SVE518T)

Concept of Multimedia, Emerging Applications, Multimedia Systems and Appliances. Distributed Multimedia Systems, Synchronization, Orchestrtion and QoS Architecture standards.

Digital audio representation and processing – Audio in computer applications, its digital representation, transmission and digital processing, speech recognition and generation. Digital video and image compression – video compression techniques and standardization of algorithms, JPEG, MPEG, DVI technology.

Multimedia Information Systems – Workstation OS, New OS support, Real Time Mach, Multimedia system service architecture, Media Stream Protocol, service and window system, client control of continuous media, Hyperapplications. Multimedia Information systems, File system support, Data Models.

Multimedia communication systems – public Network services and N/W Protocols, Quick time Movie File (QMF), format, OMFI, MHEG, Format function Real time Interchange, Track Model and Object Model Teleconferencing systems, Shared Amlication Architectures, Embedded Distributed objects, Multimedia conferencing architecture, architecture of team workstation.
Multimedia and Internet. The internet, client server technology, Communication Protocols, Internet Addressing, WWW, HTML, and Web Authoriting, Web page browsers and development, bandwidth and applications considerations, Design Considerations for Web Pages, Accessing content on internet.

BOOKS:

1. John F. Koegel Bufod: Multimedia Systems, Addison Wesley, Edition.
2. David Hillman: Multimedia Technology and Application, Galgotia Publications

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

VLSI Testing And Verification
(SVE520T)

Introduction: Introduction to Digital VLSI Design Flow Specification, High level Synthesis, RTL Design, Logic Optimization, Verification and Test Planning, Design Representation, Hardware Specific Transformations, Hardware Specific Transformations

Scheduling, Allocation and Binding: Problem Specification, Scheduling, Allocation and Binding, Basic Scheduling Algorithms (Time constrained and Resource Constrained), Allocation Steps: Unit Selection, Functional Unit Binding, Storage Binding, Interconnect Binding, Allocation Techniques: Clique Partitioning, Left-Edge Algorithm, Iterative Refinement.

Logic Optimization and Synthesis: Heuristic Minimization of Two-Level Circuits: Espresso, Finite State Machine Synthesis, Multi-Level Logic Synthesis, Multi-Level Minimization, Technology Mapping

Binary Decision Diagram: Introduction and construction, Reduction rules and Algorithms, ROBDDs, Operation on BDDs and its Algorithms, Representation of Sequential Circuits

Temporal Logic: Introduction and Basic Operators, Syntax and Semantics of LTL, CTL and CLT*, Equivalence and Expressive Power

Model Checking: Introduction to Verification, Specification and Modelling, Model Checking Algorithm, Symbolic Model Checking, Automata and its use in Verification, Practical Examples with SMV

Introduction to Digital Testing: Introduction, Test process and Test economics, Functional vs. Structural Testing Defects, Errors, Faults and Fault Modeling (mainly stuck at fault modeling), Fault Equivalence, Fault Dominance, Fault Collapsing and Checkpoint Theorem

Fault Simulation and Testability Measures: Circuit Modeling and Algorithms for Fault Simulation, (Serial Fault Simulation, Parallel Fault Simulation, Deductive Fault Simulation,Concurrent Fault Simulation), Combinational SCOAP Measures and Sequential SCOAP Measures

Combinational Circuit Test Pattern Generation: Introduction to Automatic Test Pattern Generation (ATPG) and ATPG Algebras, Standard ATPG Algorithms, D-Calculus and D-Algorithm, Basics of PODEM and FAN

Sequential Circuit Testing and Scan Chains: Introduction to BIST architecture BIST Test Pattern Generation, Response Compaction and Response Analysis, Memory BIST (March Test, BIST with MISR, Neighborhood Pattern Sensitive Fault Test), Transparent Memory BIST.

BOOKS:

1. D. D. Gajski, N. D. Dutt, A.C.-H. Wu and S.Y.-L. Lin, High-Level Synthesis: Introduction to Chip and System Design, Springer, 1st edition.
2. S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall, 2nd edition.
3. G. De Micheli. Synthesis and optimization of digital circuits, 1st edition.
4. M. Huth and M. Ryan, Logic in Computer Science modeling and reasoning about systems, Cambridge University Press, 2nd Edition.
5. Bushnell and Agrawal, Essentials of Electronic Testing for Digital, Memory & Mixed-Signal Circuits, Kluwer Academic Publishers.

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

Digital Signal processing with FPGAs
(SVE522T)

Overview of Digital Signal Processing (DSP) , Progrmmability and DSP, FPGA Technology , Classification by Granularity, Classification by Technology , FPGA and Programmable Signal Processors ,Design Implementation , FPGA Structure , , Design with Intellectual Property Cores Challenges of FPGAs.

Adders, Multipliers, Dividers, Floating-Point Arithmetic Implementation, Multiply-Accumulator (MAC) and Sum of Product (SOP), Computation of Special Functions Using CORDIC, Computation of Special Functions using MAC Calls,

Designing FIR Filters: Constant Coefficient FIR Design, Infinite Impulse Response (IIR) Digital Filters: IIR Coefficient Computation, IIR Filter Implementation, Fast IIR Filter

Multirate Signal Processing: Decimation and Interpolation ,Polyphase Decomposition, Multistage Decimator , Frequency-Sampling Filters as Band pass Decimators , Design of Arbitrary Sampling Rate Converters , Filter Banks, Wavelets

The Discrete Fourier Transform Algorithms, The Fast Fourier Transform(FFT)Algorithms, Cryptography Algorithms for FPGAs, FPGA Design of the LMS Algorithm, RTL to GDS flow case studies.

BOOKS:

1. Digital Signal Processing with Field Programmable Gate Arrays Uwe Meyer-Baese , Springer.
2. FPGA-based Implementation of Signal Processing Systems. by Roger Woods, John Mcallister, WILEY
3. VLSI Digital Signal Processing Systems: Design and implementation by Keshab K. Parhi, WILEY
4. VLSI Synthesis of DSP Kernels: Algorithmic and Architectural Transformations
5. by Mahesh Mehendale, Sunil D. Sherlekar, Kluwer Academic Publisher

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

CDMA Systems
(SVE524T)

Direct sequence and frequency hopped spread spectrum, spreading sequence and their correlation functions, Acquisition and tracking of spread spectrum signals.

Error probability for DS-CDMA, on AWGN channels, DS-CDMA on frequency selective fading channels, Performance analysis of cellular CDMA.

Capacity estimation, Power control, effect of imperfect power control on DS CDMA performance, Soft Handoffs.

Spreading /coding tradeoffs, multicarrier CDMA, IS-95 CDMA system, third generation CDMA systems, multi-user detection.

BOOKS:

1. Andrew J. Viterbi: CDMA Principles of spread spectrum communications, Addison Wesley
2. J.S. Lee and L.E. Miller: CDMA system Engineering handbook, Artech house

SCHOOL OF VLSI DESIGN AND EMBEDDED SYSTEMS
M.Tech. (VLSI Design)

VLSI Design Lab-II
(SVE504P)

Laboratory Experiments:

1. Design (using verilog), simulate and synthesize a micro-progrommed control unit of 8-bit CPU.
2. Design (using verilog), simulate and synthesize RISC architecture based 8-bit CPU .
3. Design and simulate two stage CMOS operational amplifier.
4. Design (using verilog), simulate and synthesize 8-bit Direct Digital Synthesizer.
5. Layout design of 4-bit ALU and its performance verification by simulation.
6. Layout design of a CMOS differential amplifier and its performance verification by simulation.

Note: Each experiment is expected to be completed in at least two laboratory sessions.