SCHOLL OF VLSI DESIGN & EMBEDDED SYSTEMS
NATIONAL INSTITUTE OF TECHNOLOGY, KURUKSHETRA

END-SEM EXAM SCHEDULE FOR PG

No. SVE/2020/569 Dated: 11-12-2020

Schedule of End Semester Exam of M. Tech VLSI Design and Embedded Systems

Time: Morning 10 AM onwards

Sr. No.	Date of Exam	M. Tech (VLSI Design)	Faculty Members	Date of Exam	M. Tech (Embedded Systems)	Faculty Members
1	15.12.2020	MSV 1C 01 Digital IC Design	Dr. Sudhanshu Choudhary	15.12.2020	MSV 2E 41 Digital IC Design	Dr. Sudhanshu Choudhary
2	17.12.2020	MSV 1E 43 Solid State Devices	Dr. Gaurav Verma	17.12.2020	MSV 2E 33 Introduction to MEMS	Dr. Mukesh Kumar
3	19.12.2020	MSV 1C 03 Analog IC Design	Dr. Gaurav Saini	19.12.2020	MSV 2C 13 Embedded System Software Development	Mr. Abhishek Shrimali
4	21.12.2020	MSV 1C 05 Hardware Description Languages and FPGA based Design	Prof. R. K. Sharma	21.12.2020	MSV 2C 15 Hardware Description Languages and FPGA based Design	Prof. R. K. Sharma
5	23.12.2020	MSV 1E 31 Embedded System Fundamentals	Ms. Mahak Sardana/ Mr. Abhishek Shrimali	23.12.2020	MSV 2C 11 Embedded System Fundamentals	Ms. Mahak Sardana/ Mr. Abhishek Shrimali

11/12/2020
Coordinator
School of VLSI Design & Embedded Systems

All Concerned faculty