#### NATIONAL INSTITUTE OF TECHNOLOGY KURUKSHETRA

Notification for Result of MASTER OF TECHNOLOGY IV Semester ,VLSI Design examinations November-2021

The Result of the following candidates who appeared in MASTER OF TECHNOLOGY IV Semester ,VLSI Design examination of this Institute held in November-2021 is declared as under:-

### Note: SGPA shown means Pass and "R" means Reappear

• •					
Sr. No.	Subjects				Code No.
1	Dissertation				MSV1D10
Sr. No.	Roll No.	Name	F_Name	SGPA	CGPA
1	31911228	NISHANT AVINASH DONGRE	AVINASH DONGRE	8.0000	8.9063

Title of Dissertation :

RL(A) For Result Late (Award)

Formal Techniques Used in Verification of Generic Blocks in Computer Architecture

All efforts have been made to publish this result after checking the entries properly. However, the result can stand revised in case some discrepancy is observed

Date: 2 3 NOV 2021 Kurukshetra

Prof. In-Charg

(Examinations) Reuts Reat 22/11/2021 Agrin kul 22/11/2021

# NATIONAL INSTITUTE OF TECHNOLOGY KURUKSHETRA

Notification for Result of MASTER OF TECHNOLOGY IV Semester ,VLSI Design examinations October-2021

The Result of the following candidates who appeared in MASTER OF TECHNOLOGY IV Semester, VLSI Design examination of this Institute held in October-2021 is declared as under:-

# Note: SGPA shown means Pass and "R" means Reappear

### RL(A) For Result Late (Award)

Title of Dissertation :

Sr. No.	Subjects	Code No.
1	Dissertation	MSV1D10

Sr. No.	Roll No.	Name	F_Name	SGPA	CGPA
1	31905111	MATHURTHI SANTOSH	MATHURTHI MALLESWARA RAO	8.0000	8.8438
Title of D	issertation :	Functional Verificati Chip	on of Hard Macro IPs (HM) with Aut	omation of Sy	/stem-on-
2	31907201	ANKIT CHOUHAN	RAMESH KUMAR	9.0000	8.6250
Title of D	issertation :	Exploring Physical I technology Node	ວesign Methodoiຜູງy and Implement	tation for Low	er
3	31911105	KONA SURESH	KONA SATHAIAH	9.0000	8.7188
Title of D	issertation :	Placement of Macros	s in Deep Sub Micron Technology		
4	31911211	RAHUL VIKRAM	RAJENDRA KUMAR VERMA	8.0000	8.4688
Title of Di	ssertation :	Multi-Voltage Desigr	n of RISC Processor for Low Power	Application	
5	31911212	GOUNDLA SANDHYA	SUBHANI GOUD	8.0000	8.8125
Title of Di	ssertation :	Unrolling in Fruit-v2,	, Fruit-80 and Grain128AEAD		
6	31911214	ABHISHEK KUMAR	ANIL KUMAR	9.0000	8.5781

Design and Analysis of Low Power SPAM cell

Riat A 22/11/2021

22/11/2021

7 31911215

ABHISHEK DHIMAN

K C DHIMAN

8.0000 8.5625

Title of Dissertation :

Implementation of Phase Lock Loop with Faster Locking Ability

All efforts have been made to publish this result after checking the entries properly. However, the result can stand revised in case some discrepancy is observed.

Date : 2 3 NOV 2001 Kurukshetra

Rout Jaz/11/202)