National Institute of Technology, Kurukshetra

Notification for Result of Master of Technology IV Semester School of VLSI Design and Embedded System (VLSI Design) Examinations August, 2024

The Result of the following candidates who appeared in Master of Technology IV Semester School of VLSI Design and Embedded System (VLSI Design) examination of this Institute held in August, 2024 is declared as under:-

Note: SGPA shown means Pass and "R" means Reappear

RL(A) For Result Late (Award)

Sr. No. Subjects			Code No.			
DISSER	RTATION	MSV1D10				
Roll No.	Name	Father's Name	SGPA	CGPA		
32219201	Apurv Parsodia	Yogendra Parsodia	9.0000	9.0313		
of ertation :	Performance Analysis of Power Signoff Tools To Minimize IR Drop Violations Using Power Pad Placement Technique					
32219202	Pusam Ravi Teja	Pusam Veerabhadra Rao	8.0000	8.3594		
of ertation :	Future Flow Evaluation of Standard Verification Tool (SVT)					
32219203	Jai Kishan	Babu Lal	9.0000	8.4531		
of ertation :	Optimization of Area, Timing With Trade-off Analysis in PnR Flow					
32219204	Bedanta Bikash Nath	Kumud Chandra Nath	8.0000	8.7969		
of ertation :	Power-Aware DFT Verification Algorithm in Digital Circuits					
32219205	Bovilla Madhav Reddy	Bovilla Siva Sankara Reddy	9.0000	8.3750		
of ertation :	Efficient Floor Planning for Better Timing Closure and Achievable PPA Targe with Aprisa					
32219208	Miriyala Durga Prasad	Miriayala Ramachandra Rao	9.0000	9.0156		
of sertation :	Automation for Backend Quality of Results (QoR) Improvements in Complex IoT Designs					
	DISSER Roll No. 32219201 of ertation: 32219202 of ertation: 32219203 of ertation: 32219204 of ertation: 32219205 of ertation: 32219205	Roll No. Name 32219201 Apurv Parsodia of Performance Analysis of Using Power Pad Place 32219202 Pusam Ravi Teja of Future Flow Evaluation ertation: 32219203 Jai Kishan of Optimization of Area, Tertation: 32219204 Bedanta Bikash Nath of Power-Aware DFT Verice ertation: 32219205 Bovilla Madhav Reddy of Efficient Floor Plannin with Aprisa 32219208 Miriyala Durga Prasad of Automation for Backet	DISSERTATION Roll No. Name Father's Name 32219201 Apurv Parsodia Yogendra Parsodia of Performance Analysis of Power Signoff Tools To Min	DISSERTATION Roll No. Name Father's Name SGPA 32219201 Apurv Parsodia Yogendra Parsodia 9.0000 of Performance Analysis of Power Signoff Tools To Minimize IR Drop Violentation: Using Power Pad Placement Technique 32219202 Pusam Ravi Teja Pusam Veerabhadra Rao 8.0000 of Future Flow Evaluation of Standard Verification Tool (SVT) ertation: 32219203 Jai Kishan Babu Lal 9.0000 of Optimization of Area, Timing With Trade-off Analysis in PnR Flow ertation: 32219204 Bedanta Bikash Nath Kumud Chandra Nath 8.0000 of Power-Aware DFT Verification Algorithm in Digital Circuits ertation: 32219205 Bovilla Madhav Reddy Bovilla Siva Sankara 9.0000 of Efficient Floor Planning for Better Timing Closure and Achievable PPA ertation: with Aprisa 32219208 Miriyala Durga Prasad Miriayala Ramachandra 9.0000 of Automation for Backend Quality of Results (QoR) Improvements in Co		

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7 32219209	Md Matin	Md Ahasan	9.0000	7.8750		
Title of Dissertation:	Verification of Dynamic Clock Division					
8 32219210	Shubham Saha	Uttam Kumar Saha	8.0000	8.7813		
Title of Dissertation:	Advancements in Static Timing Analysis					
9 32219213	Vimla Bharti	Arjun Prasad	8.0000	8.8750		
Title of Dissertation:	Analysis of GPU Power Consumption Across Different Milestones in ASIC Flow					
10 32219217	Piyush Bisharwal	Narendra Singh	8.0000	8.4375		
Title of Dissertation:	Design Verification of GPU Using Preemption Injection Techniques					
11 32219218	Kartik Prajapati	Ramkumar Prajapati	8.0000	8.5000		
Title of Dissertation :	Core Power Reduction	in SOC RTL and Related Desi	gn Verification T	echniques		
12 32219225	Gaurang Dinesh Shete	Dinesh Shete	8.0000	7.8125		
Title of Dissertation:	Sleep State Current Power Bi Model Across SoCs					
13 32219232	Mukund Mohan	Ramesh Chand Sharma	9.0000	7.8906		
Title of Dissertation:	Designing Robust IO Layout Taking Care of Various Layout Effects in P28 Technology					
14 32219236	Akhilesh Kumar Pal	Dina Nath Pal	8.0000	8.6719		
Title of Dissertation:	Implementation & Valid	dation of Advance Storage IPs	of Complex SO	C Design		

All efforts have been made to publish this result after checking the entries properly. However, the result can stand revised in case some discrepancy is observed.

Date:

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Faculty in Charge

Red aproduced the 4/9/24