National Institute of Technology, Kurukshetra

Notification for Result of Master of Technology IV Semester School of VLSI Design and Embedded System (VLSI Design) Examinations July, 2025

The Result of the following candidates who appeared in Master of Technology IV Semester School of VLSI Design and Embedded System (VLSI Design) Examination of this Institute held in July, 2025 is declared as under:-

Note: SGPA shown means Pass and "R" means Reappear

RL(A) For Result Late (Award)

| Sr. No. | Subjects | 3 | | Code | No. |
|------------|----------------|---|---|-------------------|---------|
| 1 | DISSER | TATION | | | MSV1D10 |
| Sr. No. | Roll No. | Name | Father's Name | SGPA | CGPA |
| 1 | 323108201 | Devang Kailashkumar Vekariya | Kailashbhai Vekariya | 9.0000 | 8.5781 |
| Title of | Dissertation | : Physical Design Implem Checks and Static Timir | nentation of RV321 RISC-V Pro ng Analysis in 45nm Open Sou | cessor with Signo | ff |
| 2 | 323108214 | Abhishek Patel | Hichchha Ram | 8.0000 | 8.5469 |
| Title of | Dissertation | RTL-TO-GDS Flow Opt | imization for Low-Power 32-BI | Γ RISC-V Process | or |
| 3 | | Shaik Waseem Burhan | Shaik Haroon Rasheed | 9.0000 | 8.7656 |
| Title of I | Dissertation : | Comprehensive Technic Design | ues for Coverage Optimization | and Verification | of SOC |
| 4 | 323408208 | Hitesh Kumar | Surinder Sharma | 8.0000 | 7.8281 |
| Title of [| Dissertation : | Physical Design Implemental Blocks on Cutting-Edge | entation for Timing Closure of Technology Node | High-Frequency I | P |

All efforts have been made to publish this result after checking the entries properly. However, the result can stand revised in case some discrepancy is observed.

Rest 05/08/2025