B.TECH. VDSE (MV) PROGRAMME SCHEME

DEPARTMENT OF VLSI DESIGN AND SYSTEMS ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY KURUKSHETRA

B.Tech in VDSE (Microelectronics and VLSI Engineering) Programme Scheme

B Tech. in VDSE (Microelectronics and VLSI Engineering) A.Y. 2026-27

SEMESTER —V

Sr. No	Course Category	Course Title	Course Code	Lecture(L)/ Tutorial(T)/ Practical(P) per week			Credits
				L	T	P	
1	PC	Linear Integrated Circuits	MVPC 301	3	1	0	3
2		Digital System Design with FPGAs	MVPC 302	3	1	0	3
3		Analog IC Design	MVPC 303	3	1	0	3
4		Digital IC Design	MVPC 304	3	1	0	3
5	OE	Open Elective-I	OE xxx	3	0	0	3
6	PC	IC Design Lab-I	MVPC 305	0	0	2	1
7		Linear Integrated Circuits Lab	MVPC 306	0	0	2	1
8		HDL lab	MVPC 307	0	0	2	1
9		Minor Project - I	MVPC 308	0	0	4	2
10		#Summer Training	MVPC 309	Six Weeks			1
11	NC	NCC/ Sports /Yoga	SWNC 101	0	0	4	2*
12	NC	NSS/Club/Technical Societies	SWNC102	0	0	4	
Total							**21**

*Continuous Evaluation Model as per guidelines and the credit to be awarded at the end of VI semester based on Cumulative performance up to VI semester.

Six-week internship after IV Semester in the summer vacation is mandatory, and it is to be evaluated in the V-Semester.

Sr.No	Course Title	Course Code
OPEN ELECTIVE-I		
1	HDL to Beginners	MVOE 301
2	Digital Logic Circuits using Logisim	MVOE 302

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SEMESTER —VI

Sr.No	Course Category	Course Title	Course Code	Lecture(L)/ Tutorial(T)/ Practical(P) per week			Credits
				L	T	P	
1	PC	Low Power Essentials	MVPC 310	3	1	0	3
2		VLSI Physical Design	MVPC 311	3	1	0	3
3		Digital VLSI Testing	MVPC 312	3	1	0	3
4	PE	Program Elective –I	MVPE xxx	3	0	0	3
5	OE	Open Elective-II	xx OE xxx	3	0	0	3
6	PC	PCB Design Lab	MVPC 313	0	0	2	1
7		IC Design Lab-II	MVPC 314	0	0	2	1
		Minor Project - II	MVPC 315	0	0	6	3
8	NC	NCC/ Sports /Yoga	SWNC 101	0	0	4	2*
9	NC	NSS/Club/Technical Societies	SWNC102	0	0	4	
Total							**20+2***

*Continuous Evaluation Model as per guidelines and the credit to be awarded at the end of VI semester based on Cumulative performance up to VI semester.

#Six-week internship during summer vacation mandatory and it is to be evaluated in VII Semester.

Sr.No	Course Title	Course Code
PROGRAM ELECTIVES - I		
1	Memory Design	MVPE 316
2	Introduction to Photonics	MVPE 317
3	Advanced Semiconductor Devices	MVPE 318
4	Digital Signal Processing for FPGA	MVPE 319
5	Information Theory and Coding	MVPE 320
6	FSM's and Real Time Applications	MVPE 321
7	MOOCs[#]	MVOC xxx
8	Courses from Industry Experts[#]	MVIE xxx

#The departmental advisory committee (DAC) will decide and float the specific MOOCs (Swayam/NPTEL) and courses from industry experts as per the latest research and industry requirements.

Sr.No	Course Title	Course Code
OPEN ELECTIVE-II		
1	Drone Systems Design	MVOE 303
2	FSM Controllers	MVOE 304

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Course Code	:	MVPC 301
Course Title	:	Linear Integrated Circuits
Number of Credits and L/T/P scheme	:	03 Credits L T P 3 0 0
Prerequisites (Course code)	:	Analog Electronics
Course Category	:	Program Core (PC)

Course Learning Objectives:

- To provide a foundational understanding of the internal structure and operation of Operational Amplifiers (Op-Amps).
- To design and analyze diverse linear and non-linear applications using op-amp ICs.
- To introduce specialized ICs including Timers, Phase Locked Loops (PLLs), and Voltage Regulators for real-world applications.

Unit I: Basics of Op-Amps: 10 hrs.

Differential Amplifiers: Analysis of DC and AC characteristics, Differential and Common-mode gains, CMRR. Op-Amp Architecture: Internal block diagram of a typical Op-Amp (IC 741), Ideal vs. Practical characteristics. DC & AC Characteristics: Input bias current, offset current, offset voltage, Slew rate, Frequency compensation, and Frequency response.

Unit II: Linear Applications of Op-Amps 10 hrs.

Basic Configurations: Inverting and Non-inverting amplifiers, Voltage follower, Summing amplifiers, and Instrumentation amplifiers. Integration and Differentiation: Ideal and Practical Differentiators and Integrators. V-to-I and I-to-V Converters: Grounded and Floating load analysis; Active Filters: Design and analysis of First and Second-order Low Pass, High Pass, Band Pass, and Band Reject filters.

Unit III: Non-Linear Applications and Oscillators 10 hrs.

Comparators: Basic comparator, Zero-crossing detector, and Schmitt Trigger (Hysteresis analysis). Precision Rectifiers: Half-wave and Full-wave precision rectifiers, Peak detectors, and Sample-and-Hold circuits. Waveform Generators: Square wave, Triangular wave, Sawtooth wave generators. Sinusoidal Oscillators: RC Phase shift, Wien Bridge, Quadrature oscillators, Hartley & Colpitts oscillators.

Unit IV: Specialized ICs and Data Converters 10 hrs.

Timer IC 555: Pin Diagram and Functional block diagram, Monostable and Astable multi-vibrator configurations. Phase Locked Loops (PLL) IC: Basic principles, Phase detector, VCO, and applications. IC Analog Multiplier, Fixed and Adjustable voltage regulators ICs, Low power design approach for sustainable linear integrated circuits applications, D-A and A-D Converters: DAC: Weighted resistor, R-2R ladder. ADC: Flash, Successive Approximation (SAR), and Dual-slope.

Course Outcomes (COs):

Upon successful completion of the course, the students will be able to:

CO1: Describe the internal blocks and characteristics of an ideal and practical Op-Amp.

CO2: Solve problems related to frequency response, compensation, and stability of linear integrated circuits.
CO3: Analyze various linear applications such as integrators, differentiators, and active filters.
CO4: Compare the performance of different Analog-to-Digital and Digital-to-Analog converters.
CO5: Design non-linear circuits such as Schmitt triggers, oscillators, and multivibrators using IC 741 and IC 555.
CO6: Examine the functionality of specialized ICs and voltage regulators.

Text/Reference Books:

[1] R. A. Gayakwad, Op-Amps and Linear Integrated Circuits, 4th ed. Upper Saddle River, NJ, USA: Pearson Education, 2015.
[2] D. R. Choudhury and S. B. Jain, Linear Integrated Circuits, 4th ed. New Delhi, India: New Age International Publishers, 2010.
[3] S. Franco, Design with Operational Amplifiers and Analog Integrated Circuits, 4th ed. New York, NY, USA: McGraw-Hill, 2014.
[4] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th ed. New York, NY, USA: Oxford University Press, 2014.
[5] R. F. Coughlin and F. F. Driscoll, *Operational Amplifiers and Linear Integrated Circuits*, 6th ed. Upper Saddle River, NJ, USA: Prentice Hall, 2001.
[6] *Linear IC Applications*, Texas Instruments (TI) Design Handbooks, Texas Instruments Incorporated, Dallas, TX, USA.

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Course Code	:	MVPC 302
Course Title	:	**FPGA-Based Digital System Design with Verilog HDL**
Number of Credits and L/T/P scheme	:	03 Credits L: 3, T: 0, P: 0
Prerequisites	:	• Fundamentals of Digital Electronics, including concepts such as logic gates, flip-flops, and finite state machines (FSMs) • Basic knowledge of Computer Organization • Understanding of Boolean Algebra and Logic Simplification
Course Category	:	PC (Program Core)

Course Objectives

- To introduce hardware description languages (HDL), focusing on Verilog
- To enable students to design and simulate both combinational and sequential circuits
- To provide understanding of FPGA architecture and design flow
- To facilitate the implementation of digital systems using Verilog on FPGA platforms
- To develop debugging and verification skills using simulation tools

Unit 1: Introduction to Verilog HDL (10 Hours)

Introduction to HDL and the different levels of design abstraction, Structure of Verilog modules, Data types in Verilog: wire, reg, integer, parameter, Operators available in Verilog, Behavioural, Dataflow, and Structural modelling techniques, Timing controls and delays in Verilog, Writing simple combinational circuits using Verilog

Unit 2: Modeling of Digital Systems (10 Hours)

Design of combinational circuits such as adders, multiplexers, encoders, and decoders, Design and modelling of sequential circuits in Verilog, including flip-flops, registers, and counters, Finite State Machines (FSM): Mealy and Moore models, Understanding blocking and non-blocking assignments in Verilog, Development of testbenches and simulation concepts, Introduction to synthesis versus simulation

Unit 3: FPGA Architecture and Design Flow (10 Hours)

Introduction to FPGA and CPLD, FPGA architecture, covering concepts such as CLBs, LUTs, routing, and I/O blocks, Overview of popular FPGA families, for example Xilinx and Intel (Altera), FPGA design flow: design entry, synthesis, implementation, and bitstream generation, Timing analysis and setting timing constraints, Introduction to FPGA development tools, such as Xilinx Vivado

Unit 4: FPGA-Based System Design & Applications (10 Hours)

Implementation of digital systems on FPGA, Memory design (RAM/ROM) using Verilog, Design of arithmetic circuits, such as ALU, Introduction to IP cores and reuse, Hardware debugging techniques, Case studies, including simple processor design and digital signal processing blocks

Course Outcomes :

Students will be able to:

1. Understand and apply Verilog constructs for digital design
2. Design and simulate both combinational and sequential circuits
3. Develop and test digital systems using testbenches
4. Comprehend FPGA architecture and the associated design flow
5. Implement and verify digital systems on FPGA platforms
6. Analyse timing and optimise hardware performance

Recommended Text-books

1. Samir Palnitkar – *Verilog HDL: A Guide to Digital Design and Synthesis*
2. Stephen Brown & Zvonko Vranesic – *Fundamentals of Digital Logic with Verilog Design*
3. Wayne Wolf – *FPGA-Based System Design*
4. Pong P. Chu – *FPGA Prototyping by Verilog Examples*
5. Michael D. Ciletti – *Advanced Digital Design with the Verilog HDL*
6. J. Bhasker, A Verilog HDL Primer, 3rd ed. Allentown, PA, USA: Star Galaxy Publishing, 2005.
7. Z. Navabi, Verilog Digital System Design, McGraw-Hill, 2017.

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Course Code	:	MVPC 303
Course Title	:	Analog IC Design
Number of Credits and L/T/P scheme	:	03 Credits
Prerequisites (Course code)	:	Semiconductor Physics, Electronic Devices and Circuits, Analog Electronics
Course Category	:	PC (Program Core)

Course objectives:

- To learn the basics of NMOS and PMOS.
- To Design and study the CMOS amplifier design.
- To understand the basics of the current mirror and bandgap reference.
- To develop the skills to design a differential amplifier and a two-stage op-amp.

Course Content

Unit - I 12 Hrs

Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second Order effects, MOS small signal Model, NMOS versus PMOS devices, single stage amplifiers, common source amplifiers with different types of loads, source follower, common-gate and common-drain amplifiers.

Unit – II 10 Hrs

Cascode stage, choice of device models, Differential amplifiers-analysis of single-ended and differential output amplifiers, common mode response, differential pair with MOS load, Gilbert cells, Frequency response of amplifiers

Unit - III 10 Hrs

Current Mirrors: Current sources and sinks, basic current mirrors, cascode current mirror, analysis of current mirrors, CMOS bandgap references: Supply independent biasing, temperature independent references, PTAT and CTAT current generation.

Unit – IV 8 Hrs

CMOS Operational Amplifiers: Performance parameters, one-stage and two-stage Op Amps, gain boosting, input range limitations, slew rate, stability, and Frequency Compensation.

Course Outcomes: At the end of the course, students will be able to

CO1: Draw the small-signal equivalent diagram of an analog circuit and analyse its performance.

CO2: Design basic amplifiers, current mirrors, differential amplifiers, bandgap reference for a given specification.

CO3: Analyse the frequency response of the different configurations of an amplifier.

CO4: understand and design CMOS Operational Amplifiers.

Text Books / Reference

1. B. Razavi, *Design of Analog CMOS Integrated Circuits*, MH.

2. P R Gray and R G Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th Edition, Wiley, 2009.

3. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Second Edition, OUP.

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Course Code	:	MVPC 304
Course Title	:	Digital IC Design
Number of Credits and L/T/P scheme	:	03 Credits L: 3, T: 0, P: 0
Prerequisites (Course code)	:	()
Course Category	:	PC (Program Core)

Course objectives:

- To learn digital integrated circuits design process.
- To understand CMOS logics, arithmetic circuits using CMOS.
- To understand and overcome power, delay and timing issues in digital ICs.

Course Content

Unit - I 12 Hrs

Introduction: MOS transistor operation, I-V characteristics, CMOS Inverter, Static and Dynamic Behavior, Power, Energy and Energy Delay, Technology scaling and its impact. Interconnect and their parameters, wire models, Effects of Interconnect Parasitic, Advanced Interconnect techniques.

Unit – II 10 Hrs

Design of CMOS Combinational Logic: Static and dynamic CMOS Design, Speed and power dissipation in dynamic circuits, cascading of gates, designing logic for reduced supply voltages.

Unit - III 10 Hrs

Design of CMOS Sequential Logic Static and dynamic latches and registers, alternative register styles, pipelined sequential circuits, non-bistable sequential circuits.

Unit – IV 8 Hrs

Custom, Semi-custom, and Structured array design approaches: Cell Based Design – standard, compiled, macro cells, mega cells, Array Based Design – mask programmable and rewired arrays. Timing issues in Digital Circuits.

Text Book:

1. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, *Digital Integrated Circuits : A Design Perspective*, Second Edition, PH/Pearson.

References:

1. S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits : Analysis and Design*, Third Edition, MH.

2. N. Weste, K. Eshraghian and M. J. S. Smith, *Principles of CMOS VLSI Design : A Systems Perspective*, Second Edition (Expanded), AW/Pearson.
3. J. P. Uyemura, *Introduction to VLSI Circuits and System*, Wiley.
4. R. J. Baker, H. W. Li and D. E. Boyce, *CMOS Circuit Design, Layout and Simulation*, PHI.

Course Outcomes: At the end of the course, students will be able to

CO1: Have an idea about Basic CMOS circuits in VLSI

CO2: Know the performance metrics of IC design.

CO3: Design integrated circuits using CMOS logic.

CO4: be able to understand power, delay and timing issues in digital ICs.

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Year/Semester	:	3rd Year / 5th Semester
Course Code	:	MVOE 301
Course Title	:	HDL to Beginners
Number of Credits and L/T/P scheme	:	L: 3, T: 0, P: 0
Prerequisites (Course code)	:	Digital Design
Course Category	:	OE (Open Elective)

Course Learning Objectives

- To introduce the concept of Hardware Description Languages (HDL) and its importance in modern digital design flow.
- To provide a foundational understanding of Verilog syntax for modeling digital hardware at different levels of abstraction.
- To develop basic skills in writing testbench programs for functional verification of digital designs.

Unit I: Introduction & Verilog Basics: **08 hrs.**

Overview: Emergence of HDLs, typical design flow, Why Verilog?; Hierarchical Modeling: Top-down vs. Bottom-up methodology, defining "Modules" and "Instances."; Basic Concepts: Lexical conventions (comments, identifiers), Data types (wire, reg, integer), and Logic values (0, 1, x, z); Modules and Ports: Defining a module, port declarations (input, output, inout), and connecting modules together.

Unit II: Behavioral Modeling 12 hrs.

Gate Primitives: Modeling logic using built-in gates (and, or, xor, not, buf); Simple Designs: Creating Half-Adders, Full-Adders, Multiplexers, Decoders, and Flip-Flops etc.; Introduction to Delays: Understanding rise, fall, and turn-off delays.

Unit III: Data-flow Modeling 10 hrs.

Continuous Assignment: The assign statement and its role in combinational logic; Expressions and Operators: Using Arithmetic (+, -), Logical (&&, ||), Bitwise (&, |), and Relational (>, <) and other operators; Operator Precedence: Solution of complex logic expressions using Verilog; Design Example: Modeling a 4-bit Magnitude Comparator and an 8-to-1 Multiplexer using data-flow, Case study.

Unit IV: Structural Modeling 10 hrs.

Structured Procedures: The initial and always blocks (how hardware reacts to changes); Procedural Assignments: Difference between Blocking (=) and Non-blocking (<=) assignments; Conditional

Logic: Using if-else and case statements, etc. for decision making; Testbenches, System Tasks ($display, $monitor), and creating a simple stimulus to check if the design works, Case study; Introduction to FPGAs; Low power design approach for sustainable digital applications.

Text / Reference Books:

i) S. Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*, 2nd ed. Upper Saddle River, NJ, USA: Pearson Education, 2003.
ii) S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with Verilog Design*, 3rd ed. New York, NY, USA: McGraw-Hill Education, 2013.
iii) M. M. Mano and M. D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog*, 6th ed. Upper Saddle River, NJ, USA: Pearson, 2017.
iv) J. Bhasker, *A Verilog HDL Primer*, 3rd ed. Allentown, PA, USA: Star Galaxy Publishing, 2005.
v) Z. Navabi, *Verilog Digital System Design*, McGraw-Hill, 2017.

Course Outcomes:

Students will be able to:

- Identify the advantages of using HDL over traditional schematic-based digital design.
- Demonstrate the use of Verilog lexical conventions and data types in hardware modeling.
- Construct structural models of digital circuits using basic gate-level primitives.
- Apply data-flow modeling and operators to design combinational logic like adders and multiplexers.
- Develop behavioral Verilog codes using procedural blocks and conditional statements.
- Perform functional verification of digital designs by writing basic testbenches and analyzing simulation outputs and gaining the basic knowledge of FPGAs.

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Course Code	:	MVOE 302
Course Title	:	Digital Logic Circuits using Logisim
Number of Credits and L/T/P scheme	:	03 Credits L T P 3 0 0
Prerequisites (Course code)	:	Digital Design
Course Category	:	OE (Open Elective)

Course Learning Objectives:

- To learn the core features and user interface of the Logisim tool for building and testing virtual fundamental digital electronic circuits.
- To design, simulate, and validate combinational building blocks, including arithmetic modules and data-routing circuits, using Logisim's analysis tools.
- To construct and evaluate sequential logic systems, memory architectures, and state-driven controllers to bridge the gap between abstract logic and practical hardware implementation.

Unit I: Digital Logic Foundations 09 hrs.

Core Concepts: Evolution of Digital Systems; Data representation and binary coding; Logic operations and the functional role of Truth Tables; Logic Gate Fundamentals: Introduction to basic gates (AND, OR, NOT) and Universal gates (NAND, NOR); Number Systems: Analysis of Positional Number Systems (Binary, Octal, Hexadecimal) and conversion techniques; Binary Arithmetic: Representation of Signed and Unsigned numbers; Operations in Signed Arithmetic; Boolean Logic: Simplification of logic functions using Sum of Products (SOP) and Product of Sums (POS) forms.

Unit II: Design of Combinational Logic Systems using Logisim 10 hrs.

Data Routing Modules: Design and simulation of Encoders, Decoders, Multiplexers (MUX), and Demultiplexers (DEMUX) in Logisim; Logic Comparators: Implementation of Parity generators/checkers and Digital Magnitude Comparators; Arithmetic Processing: Construction of binary Adders (Half/Full), Subtractors, and Multipliers; Integrated Design: Building a functional Arithmetic Logic Unit (ALU); verification of multi-bit combinational systems through graphical simulation.

Unit III: Design of Sequential Logic & Memory Elements using Logisim 11 hrs.

Basic Memory Elements: Introduction to bit-level storage; Comparative study and simulation of Latches (D-latch) and Flip-flops (D, JK, T); Data Handling Modules: Construction and verification of Shift Registers and Multi-bit Synchronous/Asynchronous Counters; Memory Architectures: Internal organization and simulation of Random Access Memory (RAM) and Read-Only Memory (ROM); System Storage: Design of Register Files for data persistence and multi-register storage units in Logisim.

Unit IV: State Machines & Processor Design using Logisim 10 hrs.

Finite State Machines (FSMs): The design workflow for Moore State Machines; creating State Diagrams and State Tables; Logic Implementation: Techniques for realizing FSMs using basic logic gates, Multiplexers, Decoders, or ROM-based lookup tables; System Integration: Introduction to simple Processor Design; combining the ALU, Registers, and Control Logic into a functional unit; Sustainable Practical Applications: Simulation of real-world controllers (e.g., Traffic Light Systems, Digital Clocks, or Vending Machines) using Logisim's clock-driven environment.

Course Outcomes:

Upon successful completion of the course, the students will be able to:

- **CO1:** Utilize binary number systems and Boolean simplification techniques to optimize digital logic functions.
- **CO2:** Demonstrate proficiency in the Logisim environment by building, testing, and troubleshooting virtual digital circuits.
- **CO3:** Construct functional combinational modules like Adders and ALUs to perform complex arithmetic and logic operations.
- **CO4:** Design sequential circuits, including counters and registers, to manage and track time-dependent data.
- **CO5:** Model and simulate Finite State Machines (FSM) to automate real-world control systems like traffic lights or vending machines.
- **CO6:** Integrate memory modules and logic blocks to explain the fundamental architecture and operation of a simple processor.

Text / Reference Books:

i) R. L. Tokheim, *Digital Electronics: Principles and Applications*, 8th ed. New York, NY, USA: McGraw-Hill, 2013.

ii) C. Burch, Logisim Reference Manual, [Online]. Available: http://www.cburch.com/logisim/docs.html.

iii) S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with Verilog Design*, 3rd ed. New York, NY, USA: McGraw-Hill Education, 2013.

iv) M. M. Mano and M. D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog*, 6th ed. Upper Saddle River, NJ, USA: Pearson, 2017.

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Course Code	:	MVPC 305
Course Title	:	IC Design Lab-I
Number of Credits and L/T/P scheme	:	01 Credits (0/0/2)
Prerequisites (Course code)	:	Electronic Devices and Circuits, Analog Electronics
Course Category	:	PC (Program Core)

Course Objectives:

- To learn the basic performance parameters and characteristics of NMOS and PMOS.
- To develop basic skills to design analog and digital VLSI circuits for a given specification.

1. Study of the basic performance parameters and characteristics of NMOS and PMOS.
2. Study the performance of the NMOS and PMOS Resistive Load Inverter.
3. Simulation of CMOS Inverter and measure its delay, Noise margin, and power dissipation.
4. Study the effect of variation in V_{DD} and W/L ratios of NMOS and PMOS transistors on the VTC of the CMOS inverter.
5. Design a 4-input NAND/NOR gate using CMOS logic and observe the effect of input transitions on the delay performance of the circuit.
6. Design and study of single-stage amplifiers (CS/CD/CG).
7. Design and study of active load single-stage amplifiers.

Course Outcomes: At the end of the course, students will be able to

CO1: Calculate basic performance parameters and characteristics of NMOS and PMOS.

CO2: Design and analyze the CMOS static and dynamic characteristics.

CO3: Measure the delay, Noise margin, and power performance of digital circuits.

CO4: Design a Common Source amplifier with different loads.

References:

1. Jan M Rabaey, Digital Integrated Circuits, 2nd Edition, Pearson Education, 2003.

2. Sung-Mo Kang, CMOS Digital Integrated Circuits, 3rd Edition, McGraw-Hill, 2003.

3. B. Razavi, *Design of Analog CMOS Integrated Circuits*, MH.

4. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Second Edition, OUP

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Course Code	:	MVPC 306
Course Title	:	Linear Integrated Circuits Lab
Number of Credits and L/T/P scheme	:	01 Credit L T P 0 0 2
Prerequisites (Course code)	:	Analog Electronics
Course Category	:	Program Core (PC)

Course Learning Objectives:

- To experimentally determine the non-ideal parameters of an Op-Amp and understand their impact on circuit performance.
- To design, breadboard, and test linear and non-linear analog circuits based on given design specifications.
- To develop the ability to diagnose and correct hardware errors in multi-stage analog systems using standard test equipment like DSOs and Function Generators.

List of Experiments:

1) To measure the Input Offset Voltage, Input Bias Current, Slew Rate, and CMRR of IC 741.
2) To design and implement Inverting/Non-Inverting Amplifiers, Adders, and Subtractors using IC 741.
3) To design and implement a Practical Integrator and Differentiator using IC741.
4) To design and implement half-wave and full-wave precision rectifiers using IC741.
5) To design and implement log/antilog amplifier using op-amp.
6) To design and plot the frequency response of a Second-Order Low Pass and High Pass Filter.
7) To design an Inverting Schmitt Trigger and measure the Upper and Lower Threshold Points to observe the Hysteresis loop.
8) To design waveform (square wave, triangular, and sawtooth) generators using IC741.
9) To design and implement a Monostable Multivibrator using IC 555.
10) To design and implement an Astable Multivibrator using IC 555
11) Project

Course Outcomes (COs):

Upon successful completion of the course, the students will be able to:

CO1: Demonstrate the ability to measure critical Op-Amp parameters such as Slew Rate, CMRR, and Offset voltages.

CO2: Analyze the performance of mathematical circuits (adders, integrators, log-amps) and compare experimental results with theoretical values.

CO3: Design and implement active filters and waveform generators for specific frequency and amplitude requirements.

CO4: Evaluate the switching characteristics and hysteresis of regenerative comparators (Schmitt Triggers).

CO5: Design and verify timing circuits using IC 555 for both one-shot (monostable) and free-running (astable) applications.

CO6: Integrate multiple ICs to build a functional prototype/project that solves a real-world engineering problem.

Text/Reference Books:

[1] R. A. Gayakwad, Op-Amps and Linear Integrated Circuits, 4th ed. Upper Saddle River, NJ, USA: Pearson Education, 2015.

[2] D. R. Choudhury and S. B. Jain, Linear Integrated Circuits, 4th ed. New Delhi, India: New Age International Publishers, 2010.

[3] S. Franco, Design with Operational Amplifiers and Analog Integrated Circuits, 4th ed. New York, NY, USA: McGraw-Hill, 2014.

[4] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th ed. New York, NY, USA: Oxford University Press, 2014.

[5] R. F. Coughlin and F. F. Driscoll, *Operational Amplifiers and Linear Integrated Circuits*, 6th ed. Upper Saddle River, NJ, USA: Prentice Hall, 2001.

[6] *Linear IC Applications*, Texas Instruments (TI) Design Handbooks, Texas Instruments Incorporated, Dallas, TX, USA.

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Course Code	:	MVPC 307
Course Title	:	HDL Lab
Number of Credits and L/T/P scheme	:	01 Credit L T P 0 0 2
Prerequisites (Course code)	:	Digital Design
Course Category	:	Program Core (PC)

Course Learning Objectives:

- To understand the syntax of Verilog HDL and the standard digital design flow, from coding to simulation and hardware implementation.
- To provide hands-on experience in designing and verifying both combinational and sequential circuits using Electronic Design Automation (EDA) tools.
- To bridge the gap between theoretical logic design and physical hardware realization using FPGA platforms and real-world peripherals.

List of Experiments:

1) To design and simulate basic logic gates using Verilog HDL.
2) To design and simulate the logic for a Half Adder and Full Adder using Verilog HDL.
3) To design and simulate a 3:8 Decoder and interface it to drive a 7-segment LED display for hexadecimal character representation.
4) To design and simulate an 8:1 Multiplexer and a 1:8 Demultiplexer to understand data routing and selection logic.
5) To design and simulate a 4-bit Magnitude Comparator using Verilog HDL.
6) To design and simulate a 4-bit Adder/Subtractor circuit using 2's complement arithmetic and carry-out detection.
7) To design and simulate various memory elements including SR, D, JK, and T Flip-Flops.
8) To design and simulate a Synchronous Mod-10 (BCD) Up-Counter.
9) To design and simulate a 4-bit Universal Shift Register for Serial-to-Parallel and Parallel-to-Serial data conversion.
10) To design and simulate a Mealy/Moore Finite State Machine (FSM) for a Sequence Detector.
11) To design, simulate, and implement a 2-bit Arithmetic Logic Unit (ALU) capable of performing 4 arithmetic and 4 logical operations on an FPGA kit.
12) Project.

Course Outcomes (COs):

Upon successful completion of the course, the students will be able to:

CO1: Explain the hierarchical modeling concepts in Verilog HDL and the synthesis process of digital hardware components.

CO2: Apply behavioral, and dataflow modeling techniques to construct combinational circuits like decoders, multiplexers, and comparators.

CO3: Implement synchronous sequential circuits including flip-flops, counters, and registers using clock-edge triggering logic.

CO4: Analyze and troubleshoot digital designs by developing comprehensive Test Benches and evaluating timing diagrams from simulation results.

CO5: Vaidate and optimize Finite State Machines (FSMs) for efficient pattern recognition and control unit operations.

CO6: Design and integrate a multi-functional system (such as an ALU) onto an FPGA platform, validating the design through physical hardware interaction.

Text/Reference Books:

i) S. Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*, 2nd ed. Upper Saddle River, NJ, USA: Pearson Education, 2003.

ii) S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with Verilog Design*, 3rd ed. New York, NY, USA: McGraw-Hill Education, 2013.

iii) M. M. Mano and M. D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog*, 6th ed. Upper Saddle River, NJ, USA: Pearson, 2017.

iv) J. Bhasker, *A Verilog HDL Primer*, 3rd ed. Allentown, PA, USA: Star Galaxy Publishing, 2005.

v) Z. Navabi, *Verilog Digital System Design*, McGraw-Hill, 2017.

Department of VLSI Design and Systems Engineering
B. Tech. in Microelectronics and VLSI Engineering

Course Code	:	MVPC 310
Course Title	:	Low Power Essentials
Number of Credits and L/T/P scheme	:	03 Credits L: 3, T: 0, P: 0
Prerequisites	:	• CMOS Technology and VLSI Design fundamentals • Semiconductor device physics (MOSFET operation) • Logic design (combinational & sequential circuits)
Course Category	:	PC (Program Core)

Course Objectives

- Understand sources of power consumption in VLSI systems
- Learn low-power design techniques at different abstraction levels
- Analyze trade-offs between power, performance, and area
- Explore modern trends and sustainability aspects in low-power design

Unit I: Fundamentals of Power Dissipation (10 Lectures)

Introduction to low-power design: Need and challenges, Power consumption in CMOS circuits: Dynamic power, Short-circuit power,Leakage power, Power dissipation mechanisms in deep submicron technologies , Power-performance trade-offs, Power estimation techniques, Activity factor and switching behaviour,

Unit II: Circuit-Level Low Power Techniques (12 Lectures)

Voltage scaling and multi-voltage design, Threshold voltage scaling, Transistor sizing for power optimization, Switching activity reduction, Adiabatic logic and energy recovery circuits , Leakage reduction techniques: Power gating, Body biasing, Multi-threshold CMOS (MTCMOS), Low-power memory design (SRAM basics)

Unit III: Architectural & System-Level Techniques (11 Lectures)

Low-power design at architectural level, Clock gating and clock distribution optimization, Power-aware RTL design, Dynamic Voltage and Frequency Scaling (DVFS), Pipeline and parallelism vs power trade-offs, Low-power interconnect design, Power management in SoCs, Low-power design automation tools overview.

Unit IV: Case Studies & Sustainability Applications (12 Lectures)

Low-power design in: Mobile devices (smartphones, wearables), IoT and edge devices , Biomedical implants, Energy-efficient processors and AI hardware, Green electronics and

sustainable VLSI design, Carbon footprint of semiconductor industry, Energy harvesting systems, Case studies: Ultra-low-power microcontrollers, Battery-operated sensor nodes, Low-power FPGA/ASIC designs, Future trends: Near-threshold computing, sub-threshold logic

Course Outcomes: Students will be able to

- Identify and quantify different sources of power consumption in CMOS circuits.
- Understand and apply circuit-level techniques to reduce both dynamic and static power.
- Learn system-level strategies for power reduction and optimization in complex ICs.
- Connect low-power design techniques with real-world applications and sustainability goals.

Textbooks

- Jan Rabaey – *Digital Integrated Circuits*
- Anantha Chandrakasan – *Low Power CMOS Design*
- Neil Weste & David Harris – *CMOS VLSI Design*

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Course Code	:	MVPC 311
Course Title	:	VLSI Physical Design
Number of Credits and L/T/P scheme	:	03 Credits L: 3, T: 0, P: 0
Prerequisites (Course code)	:	Dieital IC Design (MVPC 304)
Course Category	:	PC (Program Core)

Course objectives:

- To understand the fundamentals of VLSI physical design flow, including floor planning, placement, routing, and verification.
- To analyze design constraints such as area, power, timing, and signal integrity in deep submicron technologies.
- To develop the ability to apply algorithms and techniques for efficient placement and routing in integrated circuits.

Course Content

Unit - I 12 Hrs

Introduction: Basic concept of physical design, Layout rules & circuit abstraction, cell generation, layout environments, layout methodologies, materials for VLSI fabrication, basic algorithmic concepts for physical design, physical design processes and complexities.

Unit – II 10 Hrs

Placement: Layout compaction and its applications, design rules, symbolic layout, formulation methods, circuit representation, wire length estimation, partitioning algorithms, floor planning algorithms, placement algorithms.

Unit - III 10 Hrs

Routing: Local routing, area routing, channel routing, global routing and its algorithm, post routing optimization, reliability issues, manufacturability.

Unit – IV 8 Hrs

Key Performance Challenges in Layout Simulation and Logic Synthesis: Timing-driven placement, timing-driven routing, power minimization, physical verification and signoff, post silicon validation

Course Outcomes: At the end of the course, students will be able to

CO1: Understand techniques for block placement and partitioning during IC layout design.

CO2: Analyse and address performance issues in circuit layout design.

CO3: Apply appropriate algorithmic solutions for complex physical design problems for partitioning, floor planning, placement, and routing and clock tree synthesis.

CO4: Decompose complex mapping problems into smaller sub-problems, including logic optimization through partitioning, placement, and routing.

Text Books

Text Books:

1. M. Sarrafzadeh, “Introduction to VLSI Physical Design,” McGraw Hill (IE), 1996.

2. N. A. Sherwani, “Algorithms for VLSI Physical Design Automation,” Kluwer, 2012.

3. S. Saurabh, “ntrocduction to VLSI Design Flow” Cambridge university Press, 2023.

Department of VLSI Design and Systems Engineering
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Course Code	:	MVPC 312
Course Title	:	Digital VLSI Testing
Number of Credits and L/T/P scheme	:	03 Credits L: 3, T: 0, P: 0
Prerequisites (Course code)	:	Digital Design
Course Category	:	PC (Program Core)

Course Learning Objectives

- To learn the concepts of Digital VLSI design flow specification.
- To understand the principle of fault modeling and simulation.
- To learn ATPG algebra and algorithm for Digital VLSI testing.
- To understand the basic concept of BIST and memory testing.

UNIT-I **10hrs**

Introduction: Introduction to Digital VLSI Design Flow Specification, Brief of High-level Synthesis, Functional vs. Structural Testing, Physical faults and their modelling, Fault equivalence and dominance, fault collapsing, and Checkpoint Theorem.

UNIT II **12hrs**

Fault Simulation and Testability Measures: Circuit Modeling and Algorithms for Fault Simulation, (Serial Fault Simulation, Parallel Fault Simulation, Deductive Fault Simulation, Concurrent Fault Simulation), Combinational SCOAP Measures and Sequential SCOAP Measures.

UNIT III **10hrs**

Combinational Circuit Test Pattern Generation: Introduction to Automatic Test Pattern Generation (ATPG) and ATPG Algebras, Standard ATPG Algorithms, D-Calculus and D-Algorithm, Basics of PODEM and FAN.

UNIT IV **8hrs**

Scan Chains based Sequential Circuit Testing, Introduction to BIST architecture, BIST Test Pattern Generation, Response Compaction and Response Analysis, Memory Testing.

Course Outcomes: At the end of the course, students will be able to

CO1: Understand the difference between Design, Verification, and Test.

CO2: Understand the Physical faults and their modelling.

CO3: Understand Fault Simulation and Testability Measures.

CO4: Perform testing of combinational & sequential CMOS circuits.

CO5: Understand the concept of BIST and memory testing.

Text Books/References:

1. M. L. Bushnel and V. D. Agarwal, Essentials of Testing for Digital, Memory and Mixed – Signal VLSI Circuits, Kluwer Academic Publishers, 2000.
2. M. Abramovici, M. A. Breuer, and A. D. Friedman, Digital Systems Testing and Testable Design, IEEE Press, 1994.
3. Niraj K. Jha, Sandeep Gupta, Testing of Digital Systems, Cambridge University Press, 1st Edition, 2003.

Department of VLSI Design and Systems Engineering
B. Tech. in Microelectronics and VLSI Engineering

Memory Design
(MVPE 316)

Course Objectives:

- To learn about different types of semiconductor memories.
- To learn the fundamental problems in memory design.
- To develop novel circuit techniques for improving memory design
- To understand and appreciate the growing semiconductor market for memory

Course Content

Memory hierarchy in digital systems; Static RAM: Types, Overall architecture, SRAM Cell- Design, Layout, Noise Issues and Margins and Assembly of Core, Peripheral Circuitry - Decoding, Array conditioning for read/write, Sensing, Writing, Synchronization

Dynamic RAM: Types, Cell design, Assembly of core, Core architectures, Peripheral circuitry - Sensing, Elevated voltage supplies; Modern high speed DRAM - EDO, SDR, DDR;

Non Volatile Memories: ROM - Array Design, EPROM - Cell and Array Design, EEPROM- Tunnelling Phenomena, EEPROM Cell both Hot Carrier based operation and Tunnelling based Operation;

Flash Memories: Cell operation and design, Types of modern high density flash memories - NOR Flash, NAND Flash, Program and Erase Operation

Reference Books:

1. KiyooItoh, Masashi Horiguchi and Hitoshi Tanak, “Ultra-Low Voltage Nano-Scale Memories”’ Springer International Edition, 2007.
2. Giovanni Campardo, RinoMicheloni, David Novosel, “VLSI-Designof Non-VolatileMemories,” Springer, 2005.
3. A. K. Sharma, Advanced Semiconductor Memories : Architectures, Designs and Applications, Wiley/IEEE, 2003.
4. Betty Prince, “Semiconductor Memories: A Handbook of Design, Manufacture and Application”, 2nd Edition, John Wiley,1996.
5. Betty Prince, “High Performance Memories: New Architecture DRAMs and SRAMs – Evolution and Function”, Johm Wiley, 1999

Course outcomes

At the end of the course student will be able to

CO1: design the Semiconductor Memory architectures.
CO2: learn the fundamental problems in memory design
CO3: develop novel circuit techniques for improving memory design
CO4: understand and appreciate the growing semiconductor market for memory.

Department of VLSI Design and Systems Engineering
B. Tech. in Microelectronics and VLSI Engineering

B. Tech. in VDSE (3rd Year)
Syllabus: Introduction to photonics-MVPE-317
Credits: 3 (L–T–P: 3–0–0)

Course Learning Objectives:

- To understand fundamentals of ray, wave, and statistical optics.
- To learn photon properties and light–matter interaction, including lasers.
- To study semiconductor photonic sources and detectors.
- To introduce optical modulation, nonlinear optics, and photonic systems.

UNIT I: 8 Hrs.

Ray Optics, Wave Optics and Statistical Optics - Review of ray optics - paraxial approximation, introduction to matrix approach. Review of wave optics – interference, and diffraction of waves – Statisticalproperties of light – Spatial and Temporal coherence, Mutual coherence function - Properties of Gaussian beams.

UNIT II: 10 Hrs.

Photon properties - mean photon flux, number of photons, probability of finding a photon - Interaction of photons with atoms - absorption/emission processes - Spontaneous/stimulated emission - Optical amplification – Resonator - Laser fundamentals -Einstein Coefficients for Absorption and Emission, output power/spectrum.

UNIT III: 12 Hrs.

Semiconductor photon sources and detectors – Interaction of photons with charge carriers - LEDs - output power, spectrum, modulation characteristics – Laser diodes - threshold condition, L-Icharacteristics, longitudinal modes, modulation bandwidth - Photodiodes -Quantum efficiency & Responsivity, bandwidth –PIN and APD – gain and noise characteristics.

UNIT IV: 10 Hrs.

Manipulation of photons – Faraday effect – Basic principles of Electro optics - Nonlinear optics Stimulated Raman and Brillouin scattering, Introduction to Photonic Networks and Switching, Introduction to Optical amplifiers, and Applications of Optical Amplifiers.

Text Books:

1. Bahaa E. A. Saleh, and Malvin Carl Teich, Fundamentals of Photonics, 2nd Ed., Wiley Publishers, 2007.

Reference Books:

1. J. M. Liu, Principles of Photonics, Cambridge University Press, 2016.
2. B. G. Streetman and S. K. Banerjee, Solid State Electronic Devices, 6th Ed., Prentice Hall India Learning Pvt. Ltd, 2006.
3. A. Yariv and P. Yeh, Photonics, 6th Ed., Oxford University Press, 2006.
4. Ajoy Ghatak, Optics, 6th Ed., Mc Graw Hill Publication, 2016.
5. Eugene Hecht and A R Ganesan, Optics, 4th Ed., Pearson Education, 2014

Course outcomes (COs)

At the end of the course, students will be able to:

CO1: Analyze optical phenomena like interference, diffraction, and coherence.
CO2: Explain photon behavior and laser operation principles.
CO3: Evaluate performance of LEDs, laser diodes, and photodetectors.
CO4: Describe optical modulation, amplifiers, and photonic network applications

Department of VLSI Design and Systems Engineering
B. Tech. in Microelectronics and VLSI Engineering

Course Code	:	**MVPE-318**
Course Title	:	**Advanced Semiconductor Devices**
Number of Credits and L/T/P scheme	:	03 Credits L: 3, T: 0, P: 0
Prerequisites (Course code)	:	Electronic Devices and Circuits (ECPC 201)
Course Category	:	PC (Program Core)

Course Learning Objectives

1. To understand semiconductor fundamentals, carrier transport, and junction behaviour.
2. To study advanced MOSFET devices and short-channel effects.
3. To Analyze bipolar and heterojunction transistors for switching and high-frequency use.
4. To Explore opt-electronics devices and emerging nano-electronic technologies.

UNIT I: 10 Hrs.

Introduction of Semiconductor Devices: Introduction of Semiconductor Devices: Review of semiconductors fundamentals, Semiconductor materials and their properties, Energy bands, Carrier concentration, Fermi level, Carrier transport in semiconductors, Scattering, Defects, Phonons, mobility, Excess carriers in semiconductor, reverse recovery time, High-level injection effects.

UNIT II: 10 Hrs.

Junctions and interferences: Review of P-N Junctions, Ideal Diode Real Diode temperature dependence of I-V characteristics, Description of breakdown mechanism, Zener and Avalanche, Breakdown in P-N Junction.

UNIT III: 10 Hrs.

Advanced MOSFET Devices: Review of MOSFET operation and I-V characteristics, Short- channel effects, Silicon-on-Insulator (SOI) MOSFETs, Power MOSFETs, Heterostructure Field Effect Transistors (HFETs), Thin Film Transistor (TFT), High electron-mobility transistor (HEMT), Modulation-doped FET (MODFET).

UNIT IV: 10 Hrs.

Opto-electronics and Emerging Devices Technologies: Light-emitting diodes (LEDs), Laser diodes, semiconductor lasers, Photodetectors, and Solar cells, Nanoelectronics and quantum effects, Carbon nanotube FETs (CNTFETs).

Text Books:

2. Millman & Halkias, “Integrated Electronics”, 2nd Edition, McGraw Hill, PHI. -2017
3. S. M. Sze, “Semiconductor Devices: Physics and Technology”, 3rd Edition, John Wiley-2007

Reference Books:

6. Kevin F. Brennan, April S. Brown, “Theory of Modern Electronic Semiconductor Devices”, John Wiley & Sons, Inc, 2002, ISBN:9780471415411.
7. Robert F. Pierret, “Advanced Semiconductor Fundamentals”, 2nd Edition, Prentice Hall, 2002.
8. Karl Hess, “Advanced Theory of Semiconductor Devices”, Wiley-IEEE Press, 1999

9. Yuan Taur, Tak H. Ning, “Fundamentals of Modern VLSI Devices”, 2nd Edition, Cambridge University Press, 2013.
10. B. G. Streetman, Solid State Devices, 7th Edition, Pearson, 2016

Course outcomes (COs)

At the end of the course, students will be able to:

CO1: Explain semiconductor properties and carrier transport mechanisms.
CO2:. Understanding the concepts of P-N junctions and their interferences.
CO3: Analyse performance of advanced MOSFET devices under scaling effects
CO4: Describe operation of opto-electronics and emerging devices such as nano-electronics devices.

Department of VLSI Design and Systems Engineering
B. Tech. in Microelectronics and VLSI Engineering (Semester-VI)

Course Code	:	MVPE 319
Course Title	:	Digital Signal Processing for FPGA
Number of Credits and L/T/P scheme	:	03 Credits L T P 3 0 0
Prerequisites (Course code)	:	Signals and Systems (MVPC 203)
Course Category	:	Program Elective

Course Learning Objectives:

- To convert theoretical signal processing algorithms (Difference Equations, Z-Transforms) into efficient, synthesizable RTL code or HLS models.
- To evaluate and implement architectural trade-offs such as pipelining for throughput, folding for area-constrained designs, and retiming for low-power operation.
- To design custom fixed-point arithmetic units that balance computational accuracy with hardware resource utilization, including the management of quantization noise and bit-growth.
- To construct high-performance FIR/IIR filters and FFT engines capable of processing high-bandwidth data streams in real-time.

Unit I: FPGA Fabric & DSP Fundamentals 10 hrs.

Introduction: Evolution of DSP; FPGA vs. ASIC vs. General Purpose Processors. FPGA Architecture: Logic Elements, Interconnects, and Clock Management. Fixed-Point Arithmetic: Q-format, Word-length optimization, Truncation vs. Rounding errors.

Unit II: High-Performance Arithmetic Units 10 hrs.

Adders & Multipliers: Pipelined Carry-lookahead adders; Booth's algorithm and Wallace Tree multipliers. Timing Optimization: Critical path analysis, Retiming, and Pipelining for high-throughput. CORDIC Algorithm: Hardware implementation for Sine, Cosine, and Vector Magnitude calculations.

Unit III: Digital Filter Implementation 10 hrs.

FIR Filters: Direct, Transposed, and Systolic architectures; Polyphase decomposition. IIR Filters: Pipelining feedback loops; Cascaded Biquad structures; Stability analysis. Multirate DSP: CIC (Cascaded Integrator-Comb) filters; Interpolation and Decimation structures.

Unit IV: Frequency Domain & Transform Architectures 10 hrs.

FFT Fundamentals: Review of Radix-2/Radix-4 Butterfly structures in silicon. Memory Architectures,Windowing & DCT: Hardware for Hamming/Kaiser windows and 2D-DCT for image processing.

Course Outcomes (COs):

Upon successful completion of the course, the students will be able to:

CO1: Analyze FPGA internal resources to optimize algorithm mapping.
CO2: Design and implement fixed-point arithmetic units with proper overflow and rounding logic.
CO3: Architect high-performance FIR and IIR filters using pipelining and folding techniques.
CO4: Develop efficient FFT and CORDIC engines for frequency-domain applications.
CO5: Deploy a complete DSP system-on-chip using High-Level Synthesis (HLS).

Text/Reference Books:

1. Uwe Meyer-Baese, "Digital Signal Processing with Field Programmable Gate Arrays", 4th Edition, Springer.
2. Roger Woods, John McAllister, et al., "FPGA-based Implementation of Signal Processing Systems", Wiley.
3. Keshab K. Parhi, "VLSI Digital Signal Processing Systems: Design and mplementation", Wiley.

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Course Code	:	MVPE 320
Course Title	:	Information Theory and Coding
Number of Credits and L/T/P scheme	:	03 Credits L: 3, T: 0, P: 0
Prerequisites (Course code)	:	Communication Engineering
Course Category	:	-

Course Learning Objectives

- To understand fundamentals of Information Theory and entropy measures.
- To learn source coding techniques for data compression.
- To study channel capacity and error control coding methods.
- To introduce modern coding techniques and applications.

UNIT I: Fundamentals of Information Theory **8 Hrs.**

Introduction, Concept of information and uncertainty, Self-information and entropy, Joint entropy and conditional entropy, Markov statistical model for information source, Mutual information, Properties of entropy, Relative entropy (KL divergence).

UNIT II: **12 Hrs.**

Source Coding (Data Compression): Lossless compression techniques, Shannon's source coding theorem, Huffman coding, Shannon-Fano coding, Arithmetic coding (basic idea), Prefix codes.
Discrete Memoryless Channels: Channel models and classifications, Channel capacity, Binary symmetric channel (BSC), Shannon's channel capacity theorem, and capacity relationship.

UNIT III: **12 Hrs.**

Error Control Coding: Introduction, Need for error detection and correction, Types of error, Methods of controlling errors, Linear block codes and error correction, Generator and parity-check matrices, Hamming codes, Cyclic codes and CRC, Syndrome decoding.
Convolutional Codes & Decoding: Structure of convolutional encoders, State diagrams and trellis diagrams, Viterbi decoding algorithm, Performance analysis.

UNIT IV: **8 Hrs.**

Advanced Topics (Introductory): Turbo codes (basic idea), LDPC codes (overview), Introduction to network coding, Applications in modern communication systems (5G, data storage, IoT, VLSI).

Course outcomes (COs):

Upon successful completion of the course, the students will be able to:

CO1: Analyze and Compute entropy and mutual information.
CO2: Design and implement source coding techniques for compression.
CO3: Analyze channels capacity and implement error control codes.
CO4: Understand and interpret advanced coding methods and applications.

Text Books:

4. Thomas M. Cover, and Joy A. Thomas, “Elements of Information Theory” 2nd Edition, Wiley Inter-science, September 2006, ISBN: 978-0-471-24195-9
5. Daniel J. Costello and Shu Lin, “Error Control Coding: Fundamentals and Applications”, 2nd Edition, Pearson Prentice-Hall, April 2004, ISBN:978-0-13-042672-7

Reference Books:

11. R. Bose, “Information Theory, Coding and Cryptography”, 3rd Edition, Tata McGraw-Hill, 2016.
12. I. Csiszar and J. Korner, “Information Theory: Coding Theorems for Discrete Memoryless Systems,” Akademiai Kiado, December 1981, ISBN-13: 978-9630574402.
13. R. G. Gallager, “Information Theory and Reliable Communication” Wiley, 1968, ISBN-13: 978-0471290483
14. Simon Haykin, “Digital communication”, John Wiley, 2006.

Department of VLSI Design and Systems Engineering
B. Tech. in Microelectronics and VLSI Engineering

(FSM's and Real Time Applications)
MVPE 321

Course Objectives:

- To learn about software modelling with FSM.
- To learn the state machines for Real Time Embedded System.
- To develop novel FSM in Game AI
- To understand and appreciate FSM Applications on Communications and protocols

Course Content:

Modelling software with FSM:
UNIT I
Introduction to the Problems of software: Evolution, weakness, methods and development cycles. FSM: Defination, Notations, Hardware Applications, Software specific, designing a state machine, Systems of state machine.

UNIT II
State Works Principles and Practice: Input and outputs, Counters, Virtual FSM and its Interfaces, Debugging VFSM, Case studies: Microwave oven Control, Gas Control, Traffic Light control, Vending Machine, Pumps Supervision, Counters etc.

UNIT III
State Machines for Real-Time Embedded Systems:
Introduction to Use Case Modeling for Real-Time Embedded Systems,State Machines Examples, Events and Guard Conditions, Actions, Hierarchical State Machines, Cooperating State Machines, Inherited State Machines, Developing State Machines from Use Cases, Main Sequence and Alternative Sequences of Use Case, Develop Integrated State Machine and Hierarchical State Machine.

UNIT IV
FSM in Game AI:
A brief history of and solutions to game AI, Possibility and Probability Maps, Defining the states, Production System, Automated finite-state machines (AFSMs), Environment and AI, Animation Behaviors, Animation state machines, Smooth transitions, Navigation behaviour.

UNIT V
FSM Applications on Communications and protocols:
Implementation, Component diagrams, Spectrum of FSM Implementations, State design Pattern, Implementation based on the FSM Library: Using the FSM Library, FSM library Internals, Writing FSM Library based implementations, Examples.

Reference Books:
1. Ferdinand Wagner, Ruedi Schmuki, Thomas Wagner, Peter Wolstenholme,Modeling software with finite state machines: a practical approach, Auerbach Publications, CRC Press, Taylor & Francis Group, LLC, 2006.
2. Hassan Gomaa, Real-Time Software Design for Embedded Systems, Cambridge University Press, 2016.
3.Micael DaGraça, Practical Game AIProgramming, Packt Publishing Ltd., 2017.
4. Aung Sithu Kyaw, Clifford Peters and Thet Naing Swe, Unity 4.x Game AI Programming, Packt Publishing Ltd., 2013.
5. Miroslav Popovic, Communication ProtocolEngineering, Second Edition, CRC Press, 2018.

Course outcomes:

At the end of the course student will be able to

CO1: design the state machine and systems of state machine.

CO2: learn various FSM based case studies

CO3: develop State Machines from Use Casesfor Real-Time Embedded Systems

CO4: understand FSM in game AIand Communications protocols, and appreciate the growing market for FSM applications.

Department of VLSI Design and Systems Engineering

B. Tech. in Microelectronics and VLSI Engineering (Semester-VI)

Course Code	:	MVOE 303
Course Title	:	Drone System Design
Number of Credits and L/T/P scheme	:	03 Credits
Prerequisites (Course code)	:	Analog & Digital Communication (210), Microcontrollers & Embedded System Design (211), Control Systems (MVPC 212)
Course Category	:	Open Elective

Course Learning Objectives:

- To gain the technical proficiency to build and calibrate the hardware and flight controller components of autonomous drones.
- To Evaluate the protocols for drone-to-ground communication and the computational requirements for stable, autonomous flight.
- To Analyze how drone technology disrupts and enhances sectors such as precision agriculture, smart city infrastructure, and logistics.

UNIT I: Introduction to DroneTechnology 10 hrs.

Introduction to Drones, History of Drones, Types of Drones (Fixed-wing, Multi-rotor, Hybrid), Ethical concerns and Legal Considerations, Drone History and Evolution (Civil vs Military Applications), Flight control dynamics (Lift and Thrust, Pitch and Roll, Yaw, Translational Lift, Vortex Ring State) and basic aerodynamics of drones

UNIT II: Drone Components and Design Considerations 10 hrs.

Understanding the Drone Anatomy: How to Connect Components, understand their salient utility in drone operations, Hardware and software components: Flight Controller, PID controller using Raspberry Pi, radio controller, Implementation of advanced sensor fusion algorithms, Motors, ESCs , Power Management (Battery technology), Redundancy and Fail-safe Mechanisms Material Selection for Lightweight and Durable Drones Antennas: Patch antennas, linear antennas, and omni-directional antennas on goggles for FPV drones.

UNIT III: Communication for Drones 10 hrs.

High-frequency communication protocols and spectrum management, Comparative evaluation of wireless technologies (BLE, Wi-Fi, LoRa, ZigBee, 5G), Long-range communication technologies

(5G, mesh networks,LoRa), Drone-to-Drone communication, LOS vs BLOS operational challenges and solutions

UNIT IV: Drone Swarm Management 10 hrs.

Fundamentals of drone swarms, Swarm communication protocols, Software frameworks for swarm programming (Buzz, ROS, PaROS).

Course Outcomes (COs):

Upon successful completion of the course, the students will be able to:

CO1: Analyze the principles of flight mechanics (lift, thrust, drag) and aerodynamic forces to evaluate the performance of different drone types while ensuring compliance with global aviation laws and ethical standards.

CO2: Demonstrate the ability to design and assemble a functional drone system by integrating flight controllers, sensors (LiDAR, GPS), and power management systems, and implementing PID control loops for flight stability.

CO3: Design and evaluate robust communication frameworks for autonomous drones, selecting appropriate wireless technologies (5G, LoRa, Mesh) for Line-of-Sight (LOS) and Beyond Line-of-Sight (BLOS) operations.

CO4: Develop and simulate coordinated multi-drone missions using software frameworks like ROS and Python libraries to manage drone swarm behaviors and mission-critical task execution.

Text/Reference Books:

1. “Handbook of Unmanned Aerial Vehicles” by Kimon P. Valavanis and George J. Vachtsevanos

2. "Building Smart Drones with Esp8266 and Arduino: Build exciting drones by leveraging the capabilities of Arduino and ESP8266", by Syed Omar Faruk Towaha, CBS Publishers, 2018.

3. "Drones as Cyber-Physical Systems: Concepts and Applications for the Fourth Industrial Revolution" by Jung-Sup Um, Springer, 2019.

4. "Intelligent Autonomous Drones with Cognitive Deep Learning-Build AI-Enabled Land Drones with the Raspberry Pi 4” by David Allen Blubaugh, Steven D. Harbour, Benjamin Sears, Michael J. Findler, Springer, 2022.

5. W. Saad, M. Bennis, M. Mozaffari, and X. Lin, Wireless Communications and Networking for Unmanned Aerial Vehicles, Cambridge University Press, 2020.

6. K. Namuduri, S. Chaumette, J. Kim, and J. Sterbenz (Editors), UAV Networks and

Communications, Cambridge University Press, 2017

Department of VLSI Design and Systems Engineering
B. Tech. in Microelectronics and VLSI Engineering

Course Code	:	MVOE 304
Course Title	:	FSM Controllers
Number of Credits and L/T/P scheme	:	03 Credits L T P 3 0 0
Prerequisites (Course code)	:	MVPC 202 (Digital Design)
Course Category	:	Open Elective (OE)

Course Learning Objectives

- To understand the mathematical and logical foundations of Finite State Machines (FSM) for system modeling.
- To design and optimize synchronous and asynchronous controllers using Moore and Mealy architectures.
- To implement complex state-driven automation projects, such as sequence detectors and industrial controllers, using simulation tools.

Unit I: Foundations of State-Driven Logic 09 hrs.

From Logic to Intelligence: Limitations of combinational logic; the need for "State" and "Memory" in automation; FSM Fundamentals: Definitions of State, Inputs, Outputs, and Transitions; The Two Pillars: Detailed study of Moore vs. Mealy models; comparing output dependencies and hardware efficiency; Tools for Design: Mastering State Diagrams, State Tables, and ASM (Algorithmic State Machine) Charts.

Unit II: The FSM Design Workflow 10 hrs.

State Reduction: Techniques to minimize hardware (Row Matching and Implication Tables); State Assignment: Binary encoding, Gray coding, and One-Hot encoding; understanding the trade-off between speed and area; Excitation Logic: Deriving flip-flop input equations (D, JK, T) from state transitions; Design Example: Step-by-step construction of a 3-bit Up/Down Counter and a Modulo-N Synchronous Counter.

Unit III: Sequence Detection & Controller Logic 11 hrs.

Pattern Recognition: Design of Overlapping and Non-Overlapping Sequence Detectors (e.g., detecting "1011" in a bitstream); Advanced Sequencing: Handling "Don't Care" states and illegal state recovery (Self-Starting FSMs); Controller Implementation: Realizing FSM logic using Multiplexers, Decoders, and Programmable Logic (ROM/PLA).

Unit IV: Real-World Automation Projects 10 hrs.

Industrial Controllers: Design of a Traffic Light Controller with pedestrian sensors; Sustainable Consumer Electronics: Logic for a Digital Vending Machine (handling coins and product release); System Integration: Modeling a 4-floor Elevator Control System; handling interrupts and priority logic; The Final Step: Introduction to RTL (Register Transfer Level) design and how FSMs act as the "Control Path" for a microprocessor.

Course Outcomes:

Upon successful completion of the course, the students will be able to:

- **CO1:** Formulate state diagrams and tables to represent complex real-world logical behaviors.
- **CO2:** Compare and contrast Moore and Mealy architectures for specific design requirements.
- **CO3:** Apply state reduction and encoding techniques to optimize hardware resources.

- **CO4:** Design robust sequence detectors for communication and data processing applications.
- **CO5:** Synthesize FSM-based controllers for industrial automation tasks like traffic and elevator management.
- **CO6:** Verify the functional correctness of complex state machines through timing analysis and simulation.

Text / Reference Books:

i) R. S. Sandige, *Digital Design Essentials*, New York, NY, USA: McGraw-Hill, 2002.
ii) S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with Verilog Design*, 3rd ed. New York, NY, USA: McGraw-Hill Education, 2013.
iii) M. M. Mano and M. D. Ciletti, Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog, 6th ed. Upper Saddle River, NJ, USA: Pearson, 2017.
iv) W. I. Fletcher, *An Engineering Approach to Digital Design*, Englewood Cliffs, NJ, USA: Prentice-Hall, 1980.
v) Z. Kohavi and N. K. Jha, *Switching and Finite Automata Theory*, 3rd ed. Cambridge, UK: Cambridge University Press, 2009.

Department of VLSI Design and Systems Engineering
B. Tech. in Microelectronics and VLSI Engineering

Course Code	:	MVPC 313
Course Title	:	PCB Design Lab
Number of Credits and L/T/P scheme	:	01 Credits L–T–P: 0–0–2
Prerequisites (Course code)	:	Electronics Devices
Course Category	:	-

Course Learning Objectives

- Schematic Entry: Creating component libraries, netlist generation, and annotation.
- PCB Layout Design: Component placement, routing techniques, design rules check (DRC), and 3D visualization.
- Fabrication Techniques: Printing, etching, drilling, and soldering.
- Testing: Testing assembled PCBs for functionality.

List of Typical Experiments (Minimum 10-12)

1. Introduction to PCB DESIGN, and PCB layers, Through-hole, and SMD components, and EDA Tool Software.
2. Schematic creation of a regulated power supply (7805/7905).
3. Layout design of a voltage regulator using IC 7805.
4. Design of a Half and Full-wave rectifier.
5. PCB layout of an RC Coupled amplifier using BJT.
6. Layout of an Astable multivibrator using 555 Timer.
7. Design and fabrication of a Logic Gate circuit (e.g., AND/OR/NAND).
8. Design of an Inverting/Non-inverting amplifier using Op-Amp.
9. Automatic street light controller circuit (using LDR & Transistor).
10. Design of an IR Proximity Sensor – Touchless Door Bell using Zero PCB
11. Circuit simulation and layout of an LED flasher or Laser Light Security Alarm.
12. **Mandatory Final Project: Designing and fabricating any complex circuit (e.g., mini-project board)**

Essential Software Tools:

- Altium Designer (Industry standard)
- Autodesk EAGLE
- KiCad, EasyEda (Open source)
- OrCAD

Course outcomes (COs):
Upon successful completion of the course, the students will be able to:

CO1: Design electronic circuit schematics using EDA tools like KiCad or EAGLE and verify them using ERC.

CO2: Develop PCB layouts by applying component placement, routing techniques, and design rules, and generate fabrication files (Gerber files).
CO3: Fabricate, assemble, and test PCB prototypes using appropriate soldering techniques and debugging methods.

Text Books:

1. Simon Monk, “Make Your Own PCBs with EAGLE: From Schematic Designs to Finished Boards (Electronics)” 2017

Reference Books:

1. S. Yogesh, “OSCAD: An Open-source EDA Tool for Circuit Design, Simulation, Analysis and PCB Design”, Shroff Publishers & Distributors Pvt. Ltd, 2013.
2. Michael D. Smith, Practical Pcb Design: A Hands-on Guide to Developing Printed Circuit Boards, 2026.

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Course Code	:	MVPC 314
Course Title	:	IC Design Lab-II
Number of Credits and L/T/P scheme	:	01 Credits (0/0/2)
Prerequisites (Course code)	:	EDC, Analog Electronics, AIC, DIC
Course Category	:	PC (Program Core)

Course Objective:

To develop advanced skills in designing digital, analog, and mixed-signal VLSI circuits to meet specified requirements.

1) Design and study of a basic CMOS current mirror.
2) Design and study of a CMOS differential amplifier with different loads.
3) Design and optimize a two-stage CMOS operational amplifier.
4) Design and study of band-gap voltage reference.
5) Design and study of CMOS-based 1-bit 6T SRAM cell.
6) Layout of CMOS Inverter/NOR/NAND gate, and perform post-layout simulation.

Mini Projects: PLL, LDO, LNA, Mixer, ADCs, oscillators, filters, DC-DC converters, etc.

Note: Each experiment is expected to be completed in at least two laboratory sessions.

Course Outcomes: At the end of the course, students will be able to

CO1: Design basic CMOS current mirrors.
CO2: Design and optimize differential amplifiers and a two-stage op-amp.
CO3: Design and evaluate the performance of a 6T-SRAM cell.
CO4: Design bandgap reference circuits.
CO5: Perform post-layout simulation of CMOS inverter.

References:

1. Jan M Rabaey, Digital Integrated Circuits, 2nd Edition, Pearson Education, 2003.

2. Sung-Mo Kang, CMOS Digital Integrated Circuits, 3rd Edition, McGraw-Hill, 2003.

3. B. Razavi, *Design of Analog CMOS Integrated Circuits*, MH.

4. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Second Edition, OUP.